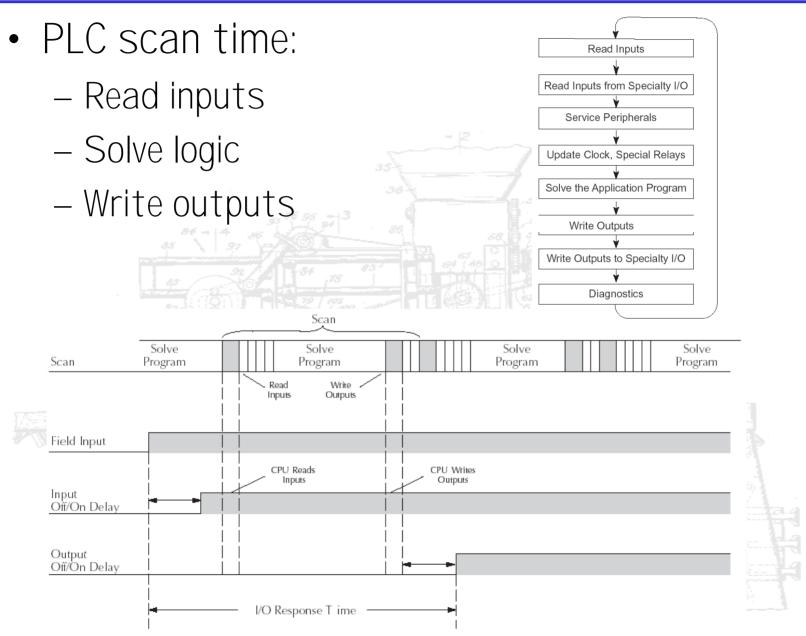
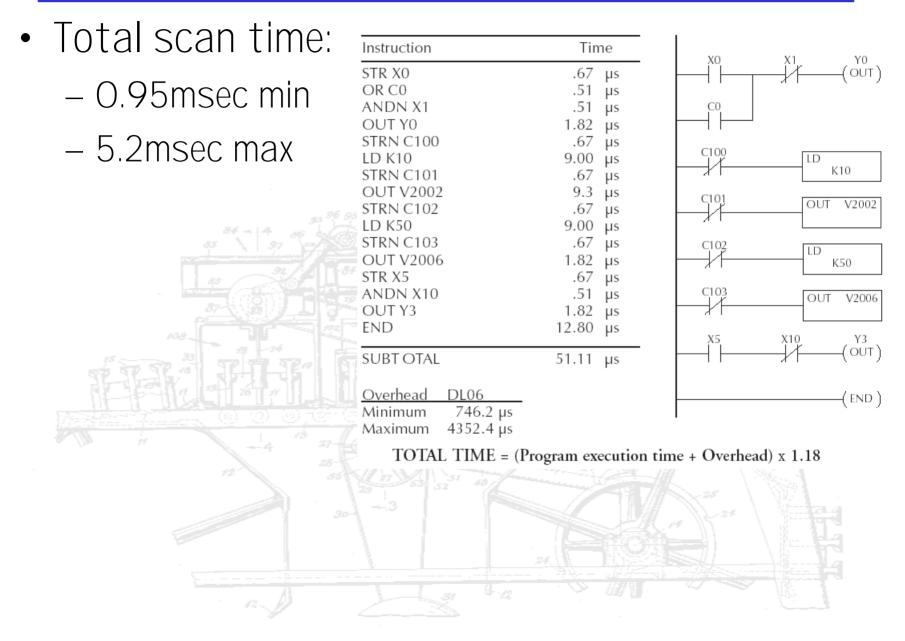
Proportional Control with the PLC

- High Speed Input
- Pulse Output
- PID control

PLC Input/Output Timing

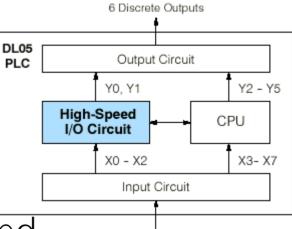


PLC Input/Output Timing



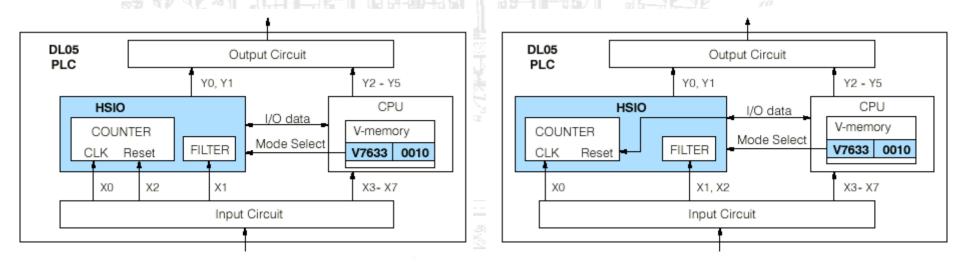
High Speed Input/Output

- High speed counters
 Use XO,X1, and X2
- Pulse Output
 Uses YO and Y1
- One of six modes can be used
 Mode 10: High speed counter
 Mode 20: Quadrature counter
 - Mode 30: Pulse Output
 - Mode 40: High speed interrupt
 - Mode 50: Narrow pulse capture
 - Mode 60: Narrow pulse reject (normal mode)

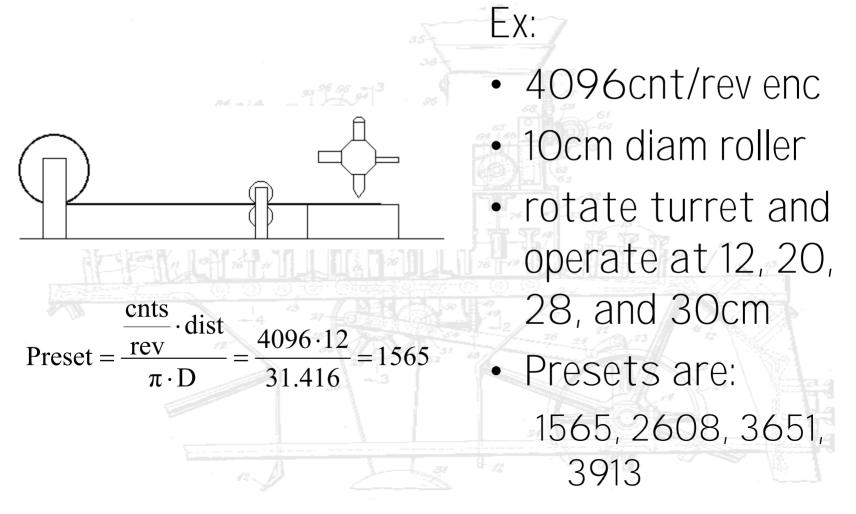


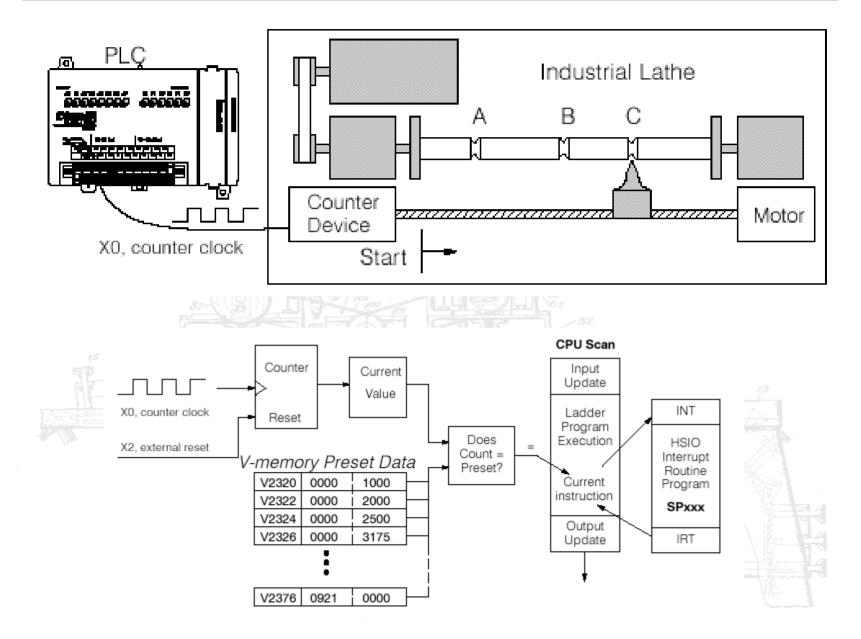
8 Discrete Inputs

- Up counter, counts to 99,999,999
- Up to 5kHz input rate (incr. on XO low->hi)
- Count is compared to preset values to generate events.
- Reset can be X2 or ladder logic



Used for applications like cut-to-length

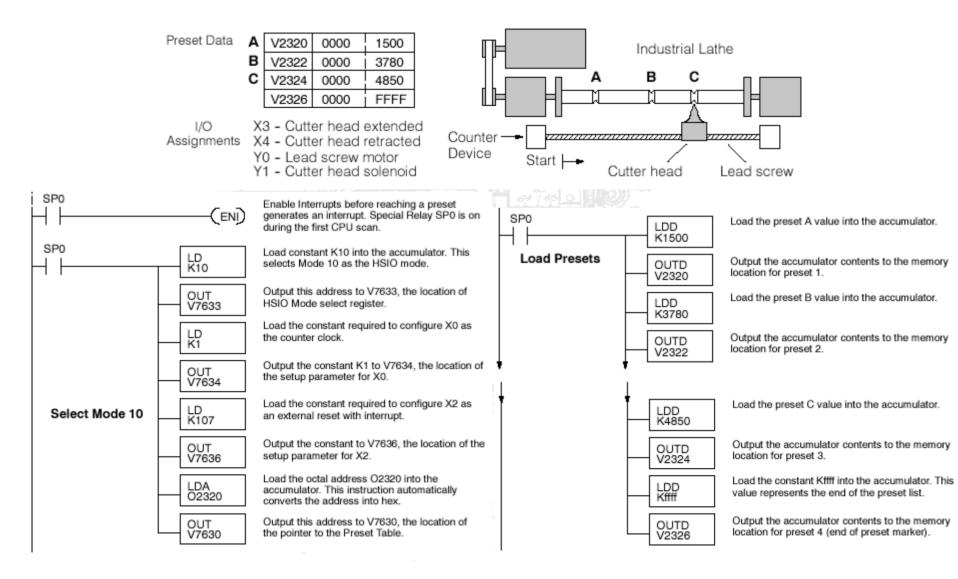


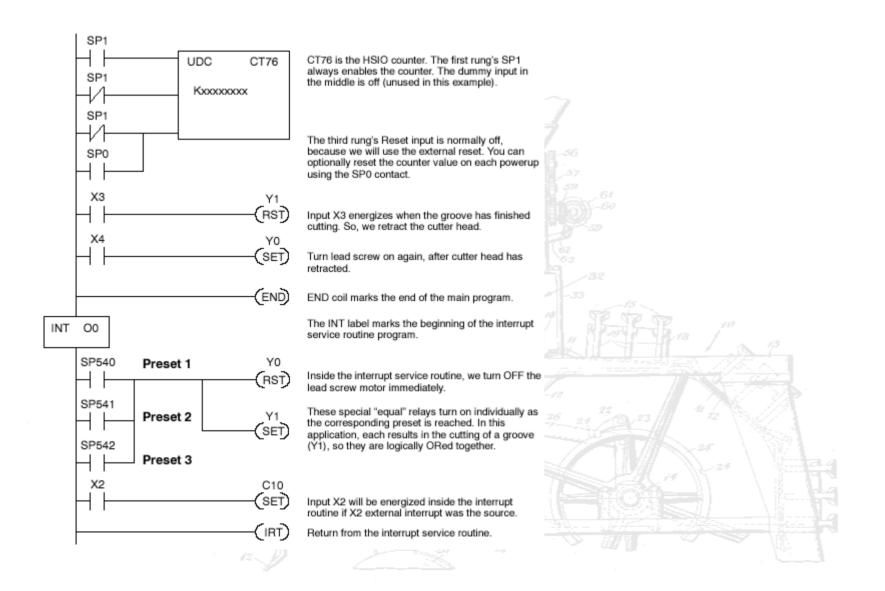


 Setup consists of writing values to several special memory locations

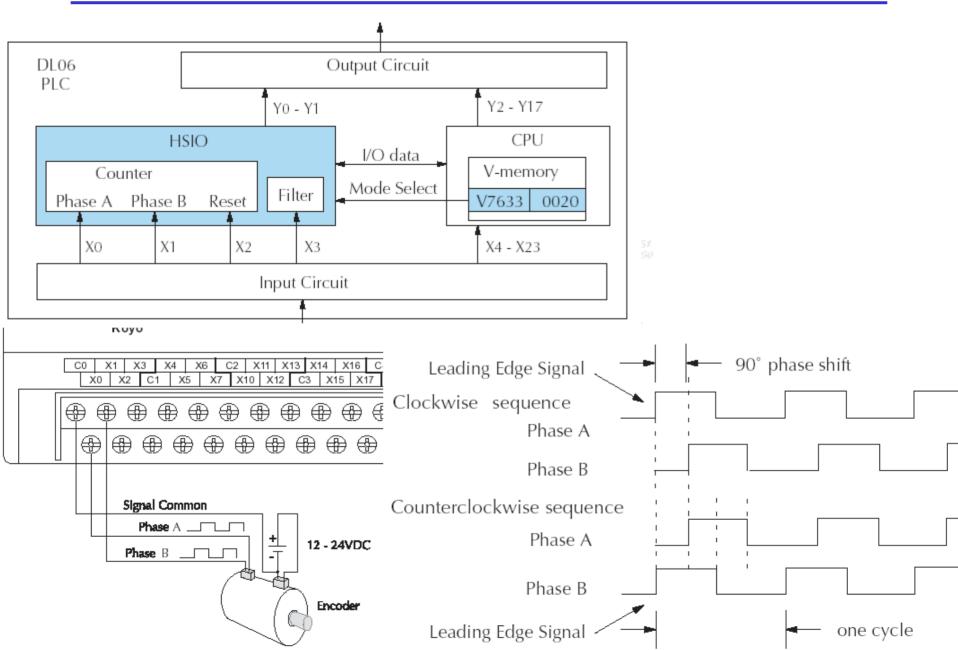
Input	Configuration Register	Function	Hex Code Required
X0	V7634	Counter Clock	0001
X1	V7635	Filtered Input	xx06, xx = filter time 0 - 99 ms (BCD)
X2	V7636	Counter Reset (no interrupt)	0007* (default) 0207*
		Counter Reset (with interrupt)	0107* 0307*
		Filtered Input	xx06, xx = filter time 0 - 99 ms (BCD)

Preset	Preset V-memory Regis- ter	Special Relay Number	Preset	Preset V-memory Regis- ter	Special Relay Number
1	V2321 / V2320	SP540	13	V2351 / V2350	SP554
2	V2323 / V2322	SP541	14	V2353 / V2352	SP555
3	V2325 / V2324	SP542	15	V2355 / V2354	SP556
4	V2327 / V2326	SP543	16	V2357 / V2356	SP557
5	V2331 / V2330	SP544	17	V2361 / V2360	SP560
6	V2333 / V2332	SP545	18	V2363 / V2362	SP561
7	V2335 / V2334	SP546	19	V2365 / V2364	SP562
8	V2337 / V2336	SP547	20	V2367 / V2366	SP563
9	V2341 / V2340	SP550	21	V2371 / V2370	SP564
10	V2343 / V2342	SP551	22	V2373 / V2372	SP565
11	V2345 / V2344	SP552	23	V2375 / V2374	SP566
12	V2347 / V2346	SP553	24	V2377 / V2376	SP567





Mode 20 Quadrature Counter



Mode 20 Configuration

Input	Configuration Register	Function	Hex Code Required	DirectSOFT32 (ENI)	
XO	V7634	Up counting	0202 (standard, absolute) 0302 (standard, incremental)		Load constant K20 into the accumulator . This selects Mode 20 as the HSIO mode.
		Phase A	0002 (quadrature, absolute) (default) 0102 (quadrature, incremental) 1002 (quadrature, absolute) 4x counting*	OLIT V7633	Output this address to V7633, the location of the HSKO Mode select register . Load the constant required to configure XD as a
	1/2005		1102 (quadrature, incremental) 4x counting*	К2	quadrature absolute input.
X1	V7635	Down counting or Phase B	0000	OUT V7634	Output the constant to V7634, the location of the setup register for XO.
		Counter Reset (no interrupt)	0007** (default) 0207**		Load the constant required to configure X2 as an external reset with interrupt.
X2	V7636	Counter Reset (with interrupt)	0107** 0307**	OUT V7636	Output the constant to V7636, the location of the setup register for X2.
		Pulse input	0005		Load the constant required to configure X3 as a filtered
		Filtered input	xx06 (xx = filter time, 0 - 99ms (BCD)	LD K2006	input.
Х3	V7637	Pulse input Filtered input	0005 xx06 (xx = filter time, 0 - 99ms (BCD) (default)	OUT V7637	Output the constant to V7637, the location of the setup register for X3.
		87-12 188		LDD Ksooo	Load the preset 1 value into the accumulator.
Stand	lard Counter Fu	nction	OUTD V3630	Output the accumulator contents to the memory location for preset 1.	
UP Cot	unt UDC	CTxx	Enable Input UDC CT174		Load the constant required to configure XD as Phase A input.
DOWN Count		Preload Input		OUID V3632	Output the constant to V7634, the location of the setup register for XO.
Reset Ir	1put	Reset Input		LDD K15000	Load the constant required to configure X1 as Phase B input.
Counts UP and DOWN Counts UP and DOWN (from X0, X1)				OUID V3634	Output the constant to V7635, the location of the setup register for X1.
	ad counter by write input is internal or			LDD KEFFF	Load the constant required to configure X2 as an external reset.
				OUID V3636	Output the constant to V7636, the location of the setup register for X2.
		ين 19540 م 1	Set Y0 to ON when the counter reaches or exceeds our comparison value while COUNTING UP Set Y1 to ON when the counter reaches or goes below our comparison value while COUNTING DOWN.	SP1 UDC CT 174 SP1 K18724	CT174 is the HSIO quadrature counter. The first rung's SPI always enables the counter . The dummy input is used by the built-in compiler
			our comparison value while COUNTING DOWN.		END coil marks the end of the main program