HW #1

16.1 (a) $R_{on} = r_{DSN}$

$$= \frac{1}{(\mu_n C_{ox})\left(\frac{W}{L}\right)_n (V_{DD} - V_{tn})} \quad (1)$$

$$= \frac{1}{0.540 \times 1.5(1 - 0.35)} = 1.90\ \text{k}\Omega$$

(b) $R_{on} = r_{DSP}$

$$= \frac{1}{(\mu_p C_{ox})\left(\frac{W}{L}\right)_p (V_{DD} - |V_{tp}|)} \quad (2)$$

$$= \frac{1}{0.100 \times 1.5(1 - 0.35)} = 10.26\ \text{k}\Omega$$

(c) From (1) and (2) since $V_{tn} = -|V_{tp}|$, then if R_{on} are to be equal, then

$$(\mu_n C_{ox})\left(\frac{W}{L}\right)_n = (\mu_p C_{ox})\left(\frac{W}{L}\right)_p$$

$$\Rightarrow \left(\frac{W}{L}\right)_p = \frac{\mu_n C_{ox}}{\mu_p C_{ox}}\left(\frac{W}{L}\right)_n$$

$$= \frac{540}{100} \times 1.5 = 8.1$$

16.6

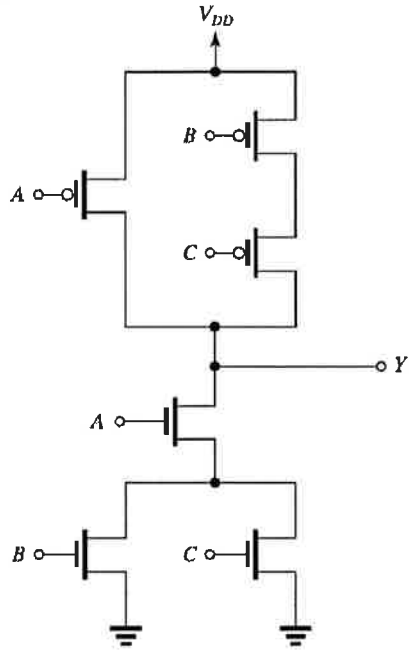

Figure 1

Figure 1 shows the complete CMOS circuit where the PUN is obtained as the dual network of the given PDN. The logic function realized can be written from the PDN as

$\overline{Y} = A(B + C)$

or equivalently

$Y = \overline{A(B + C)}$

16.7

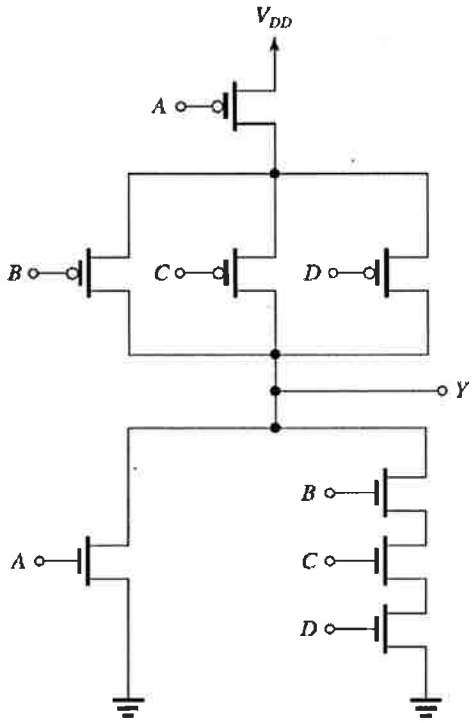

Figure 1

Figure 1 shows the complete CMOS logic circuit where we have obtained the PDN as the dual of the given PUN. The logic function can be written from the PDN as

$\overline{Y} = A + BCD$

or equivalently

$Y = \overline{A + BCD}$

16.11 Direct realization of the given expression results in the PUN of the logic circuit shown in Fig. 1. The PDN shown is obtained as the dual of the PUN. Not shown are the two inverters needed to obtain $\overline{A}$ and $\overline{B}$.

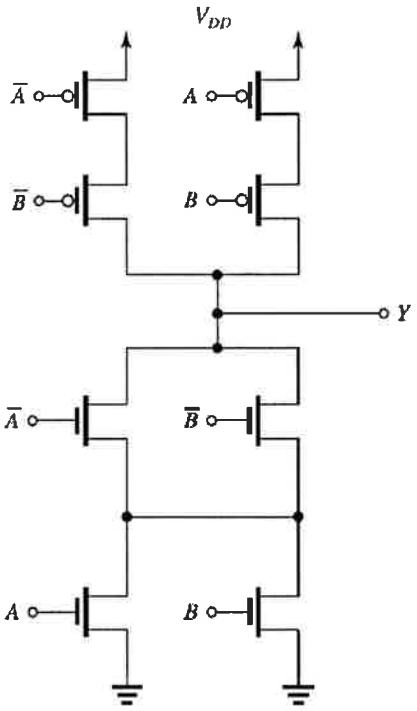

Figure 1

16.18 $NM_H = V_{OH} - V_{IH}$

$= 0.8V_{DD} - 0.6V_{DD} = 0.2V_{DD}$

$NM_L = V_{IL} - V_{OL}$

$= 0.4V_{DD} - 0.1V_{DD} = 0.3V_{DD}$

Width of transition region $= V_{IH} - V_{IL}$

$= 0.6V_{DD} - 0.4V_{DD} = 0.2V_{DD}$

For a minimum noise margin of 0.25 V, we have

$NM_H = 0.25$

$\Rightarrow 0.2V_{DD} = 0.25$

$\Rightarrow V_{DD} = 1.25$ V

16.19 (a) Refer to Fig. 16.17.

$$V_{OL} = V_{DD}\frac{R_{on}}{R + R_{on}}$$

$$= 1.8 \times \frac{0.1}{2 + 0.1} = 0.086 \text{ V}$$

$$V_{OH} = V_{DD} = 1.8 \text{ V}$$

$$NM_H = V_{OH} - V_{IH}$$

$$= 1.8 - 0.8 = 1 \text{ V}$$

$$NM_L = V_{IL} - V_{OL}$$

$$= 0.6 - 0.086 = 0.514 \text{ V}$$

(b) Refer to Fig. 1.

$$V_{OH} = V_{DD} - N \times 0.1 \times R$$

$$= 1.8 - N \times 0.1 \times 2$$

$$= 1.8 - 0.2N$$

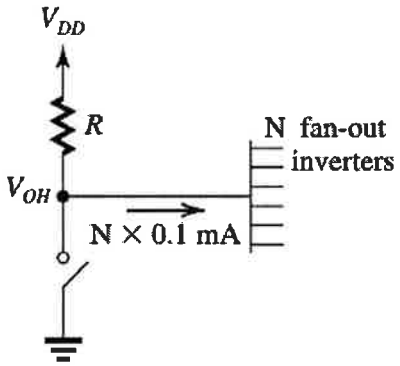

Figure 1

$$NM_H = 1.8 - 0.2N - 0.8$$

$$= 1 - 0.2N$$

For $NM_H \geqslant NM_L$, we have

$$1 - 0.2N \geqslant 0.514$$

$$\Rightarrow N \leqslant 2.43$$

which means

$$N = 2$$

(c) (i) When the inverter output is low,

$$P_D = \frac{V_{DD}^2}{R + R_{on}} = \frac{1.8^2}{2 + 0.1} \simeq 1.54 \text{ mW}$$

(ii) When the output is high and the inverter is driving two inverters, the current drawn from the supply is $2 \times 0.1 = 0.2$ mA and thus the power dissipation is

$$P_D = V_{DD} I_{DD} = 1.8 \times 0.2 = 0.36 \text{ mW}$$