

## Notes regarding 8x16 LED display board operation and testing

### Operation

The 8x16 LED display board uses a multiplexing scheme where only one LED out of the 128 is turned on at a time. An 8x16 bit memory array is placed in the FPGA and then one bit at a time is sent to the display along with a 7-bit address (total of 8 parallel bits). The complete 128 bit sequence is repeated about 78 times per second. At that rate, the eye integrates the quickly flashing LEDs and it appears as if LEDs are constantly on.

### Driver circuit

A VHDL description of a driver circuit is available on the class web page. This circuit has the 8x16 bit memory (16 8-bit words), a display clock generator, and a multiplexer circuit that selects one bit at a time to send. The file name is “led\_8x16\_driver.vhd”. 8-bits (one column) at a time of data is written to the display memory when the write enable (we) signal is asserted and a positive clock edge occurs on the clock input (a clock typically coming from the user’s circuit).

### Display test circuit

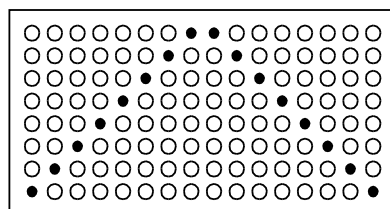
A test circuit is available for downloading into the FPGA to confirm that connections between the FPGA and the display circuit are correct. Two files are posted. Use the one matching the specific Spartan6 daughter board you are using. The text on the class web page for this file is:

Circuit to test 8x16 LED display (two versions, for FPGA boards with sdram or ddr3)

File names are:        test\_led\_display\_fpga3\_sdram.bit  
                         or    test\_led\_display\_fpga3\_ddr3.bit

To use this test circuit, connect the 8 signal lines from display to extout on the FPGA board as well as ground and 3 volts. Download the .bit file to your account. If you don’t have the Xilinx ISE-14 tools running you can start Impact by itself by typing impact in a terminal window and select the bit file as the configuration file. Download as normal. Or, if you have ISE14 running you can start Impact from within, select the desired bit file, and download.

After configuring the FPGA this lamp pattern should be observed (block dots are lit LEDs):



Press sw13 and the display will become dynamic. One lit LED will scan across all the LED positions column by column, bottom to top, left to right, leaving the top row of LEDs on. Pressing sw13 again will stop the scanning, press again and it will resume but not at the same location as where it stopped (and you can end up with LEDs temporarily on until the next scan cycle, that is normal).

See also “8x16 display connection details” (file led\_8x16\_display\_details.pdf) on engr433 web page.