Further Consideration of State Machine Operation

Three topics today

- More detail about basic flip-flops
- State machine next state logic design
- State machine timing





Recall the resolver circuit for creating an edge triggered F/F and creation of the next state logic where the state number is binary encoded:



Next state logic design using one-hot encoding The state number, in binary, is all zeros except one digit is a one



Here is the same state diagram with branching conditions added



Formal definition of one-hot encoding



Below are equations that summarize next state logic D and output logic Z

$$D_j = \sum_{k=0}^{m-1} Q_k \cdot f_{j \leftarrow k}$$
 and $Z_l = \sum_{j=0}^{m-1} Q_j \cdot f_{j,l}(X)$.

For the four-state example, here is the circuit:



Here is the logic for each state bit.



NEXT STATE LOGIC

$$D_a = \overline{X} Q_a + Q_d$$

 $D_b = \overline{X} \overline{Y} Q_a$
 $D_c = \overline{X} Y Q_a + S Q_b + \overline{X} Q_c$
 $D_d = \overline{S} Q_b + \overline{X} Q_c$

One-hot plus one state coding: Adds an initial state to force transition to a desired state at system start-up.



A more complex example.

