Digital Design Intro

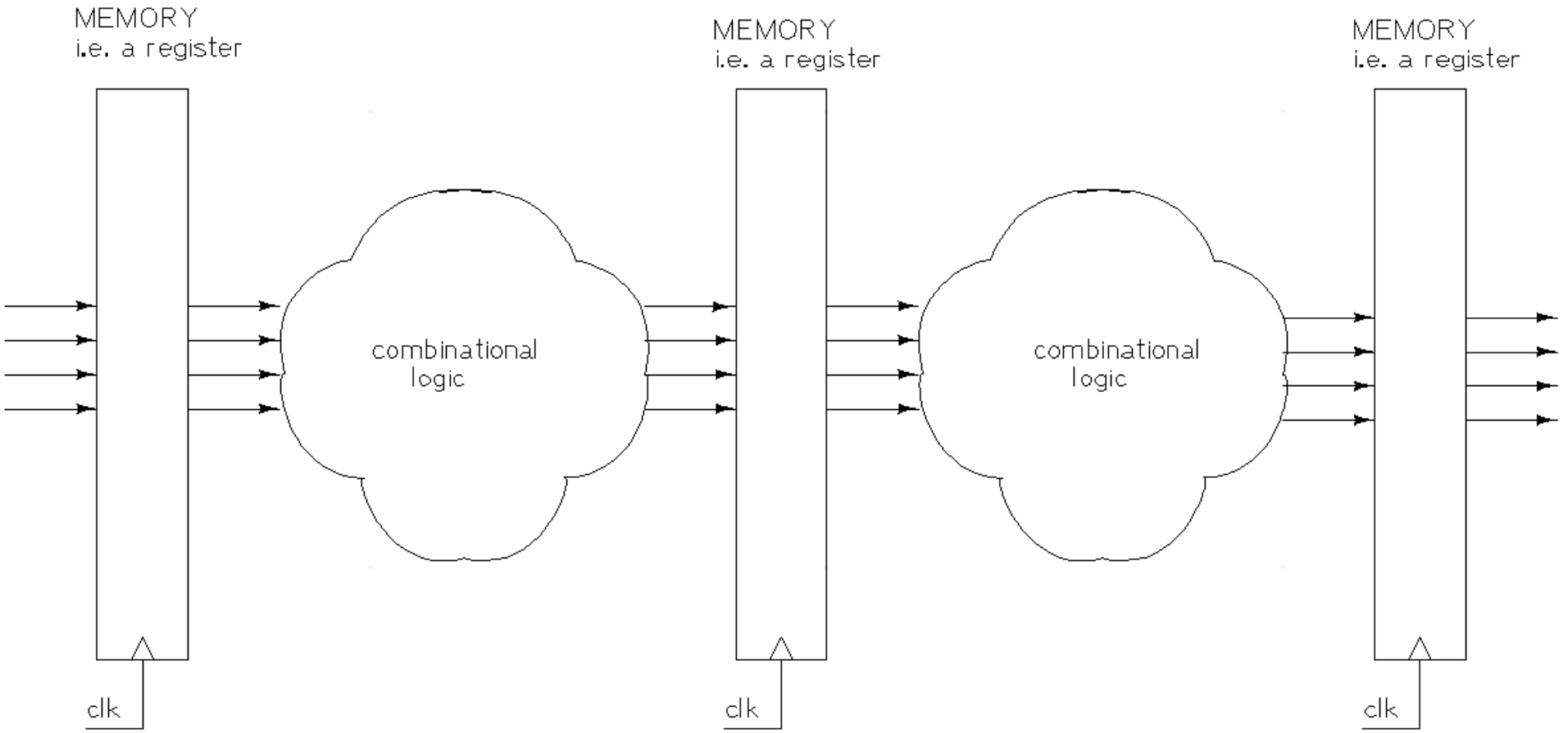
Today: an introduction and a bit of review

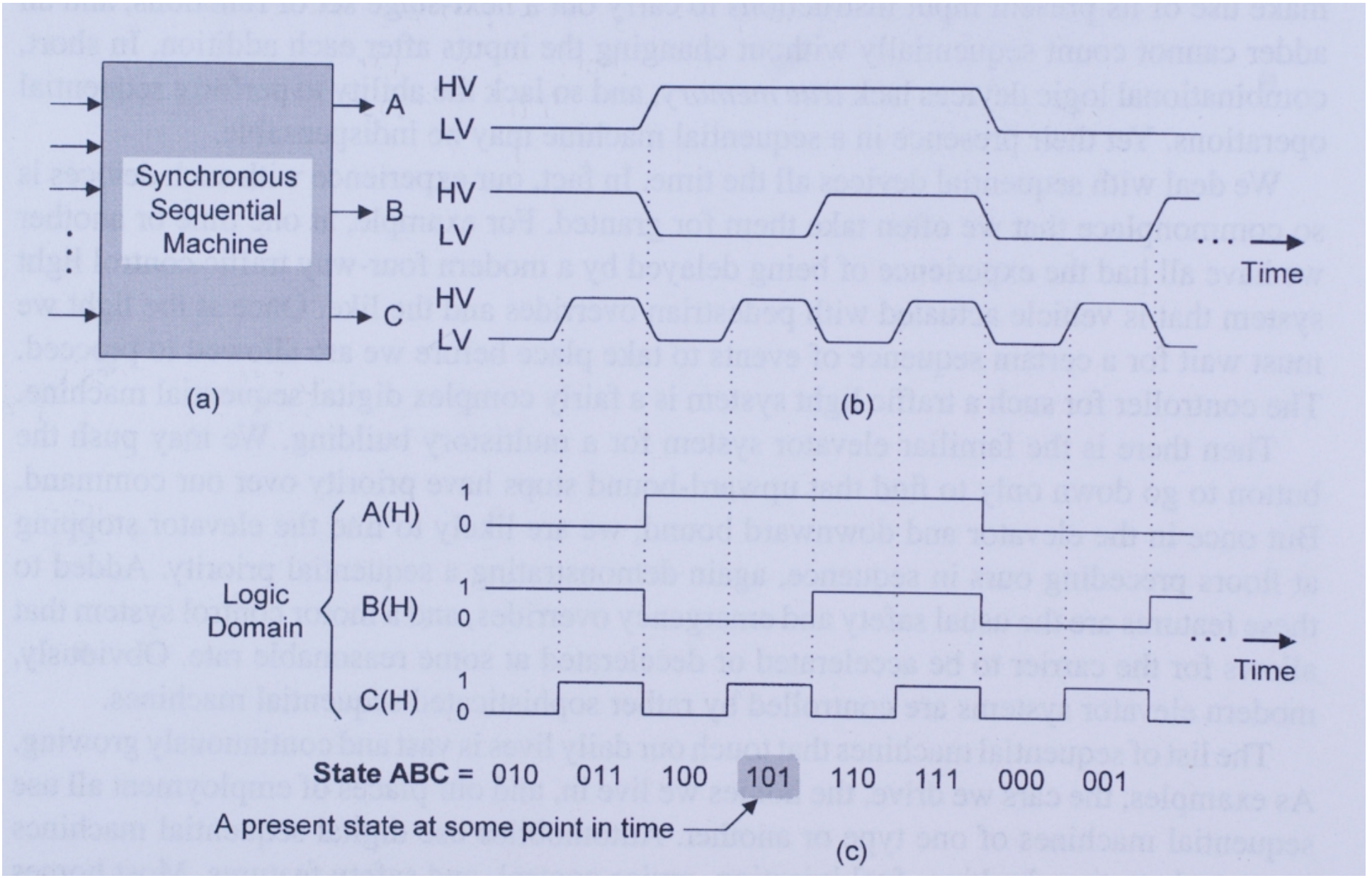
- What this course is about
- Basic digital logic
- State machines
  - architecture of a state machine circuit
  - documentation of state machine operation
  - fundamentals of memory
  - synchronous finite state machine (FSM)
- Lab planning

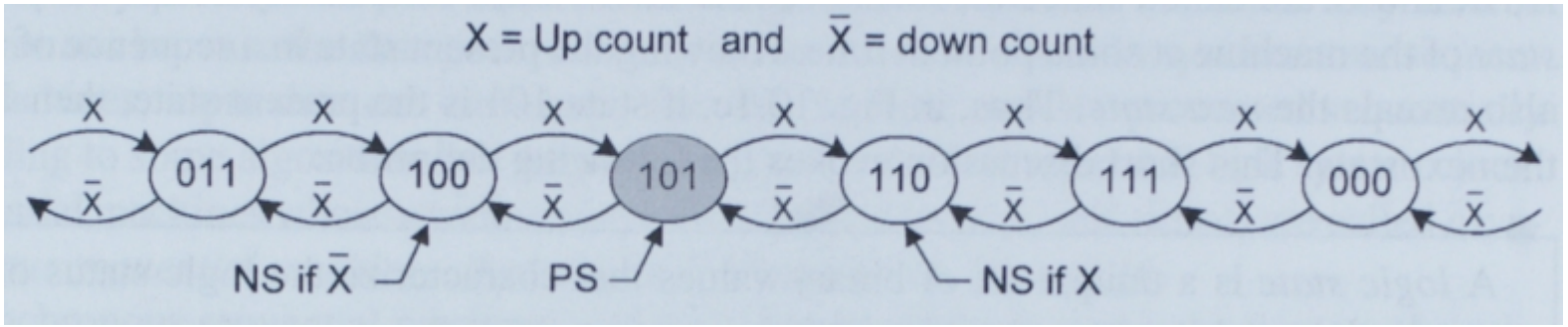
Class topics

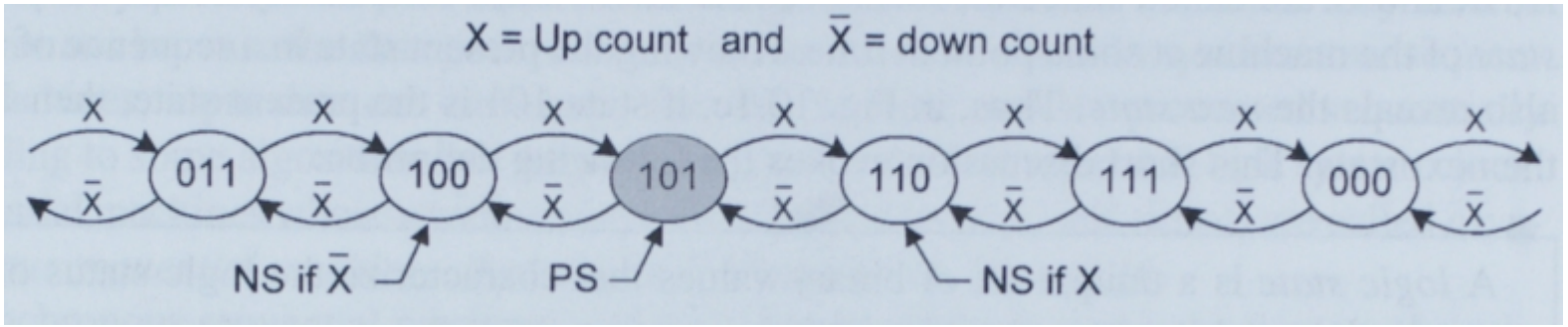
- basics of memory
- logic circuit building blocks
    - logic gates
    - multiplexers
    - decoders
    - counters
    - comparators
- finite state machines (FSM)
- VHDL language basics
- VHDL circuit descriptions for synthesis
- logic hazards and pitfalls
- electrical design of digital circuits
- Field Programmable Gate Arrays (FPGAs)
- Use of a design tool (Xilinx ISE)

RTL – Register Transfer Level circuit description




Synchronous Sequential Machine
A
B
C
(a)
HV
LV
HV
LV
HV
LV
Time
(b)
Logic Domain
A(H)
B(H)
C(H)
1
0
Time
State ABC = 010 011 100 101 110 111 000 001
A present state at some point in time
(c)


X = Up count and $\bar{X}$ = down count
X
$\bar{X}$
011
100
101
110
111
000
NS if $\bar{X}$
PS
NS if X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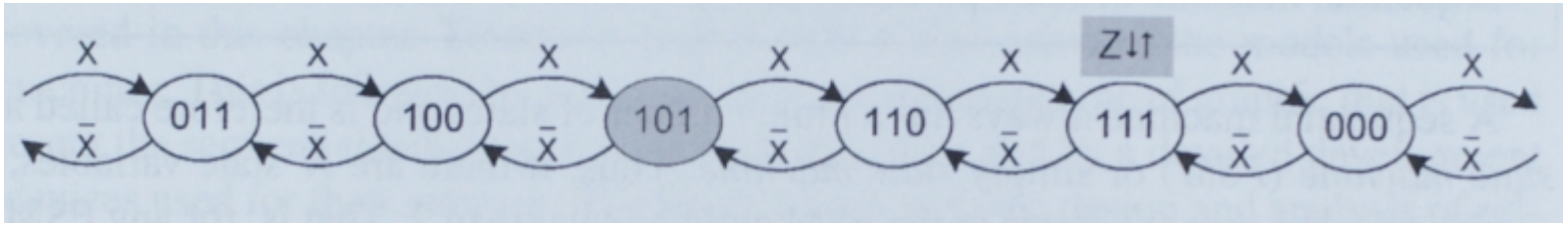
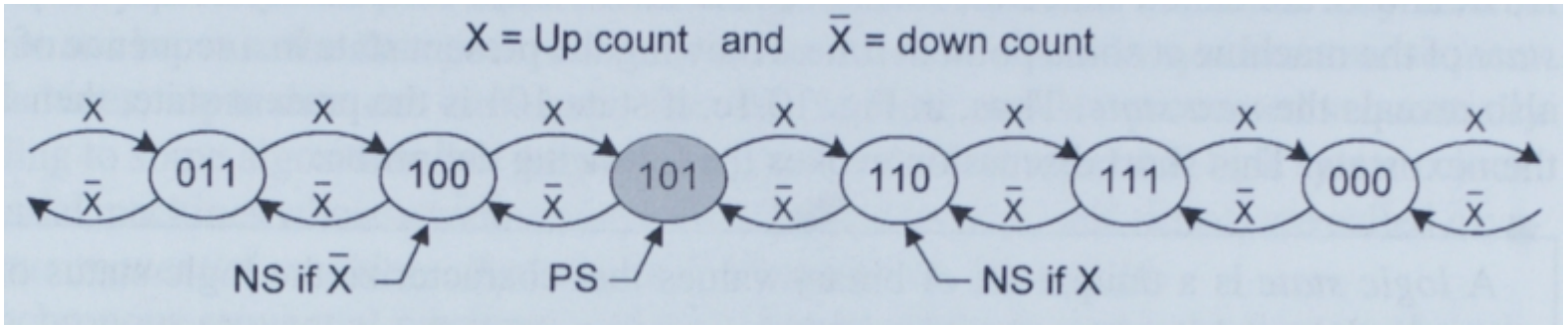

Z↓↑
X
$\bar{X}$
011
100
101
110
111
000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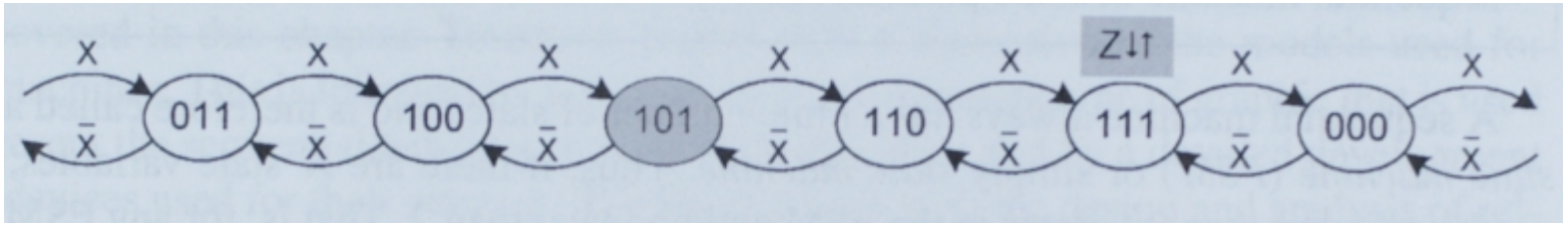
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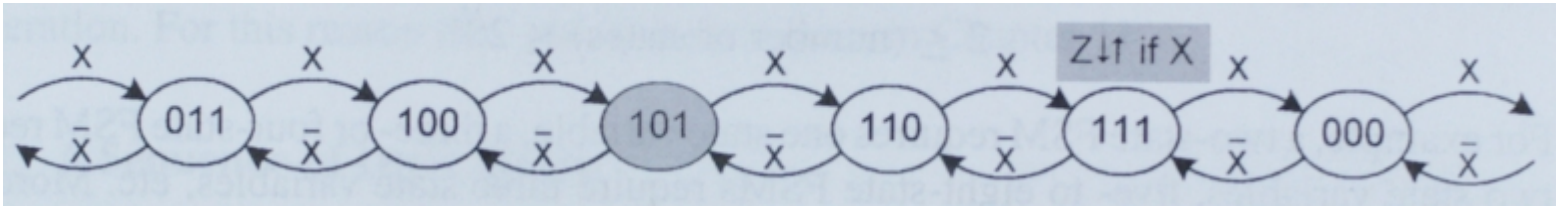
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$\bar{X}$
011
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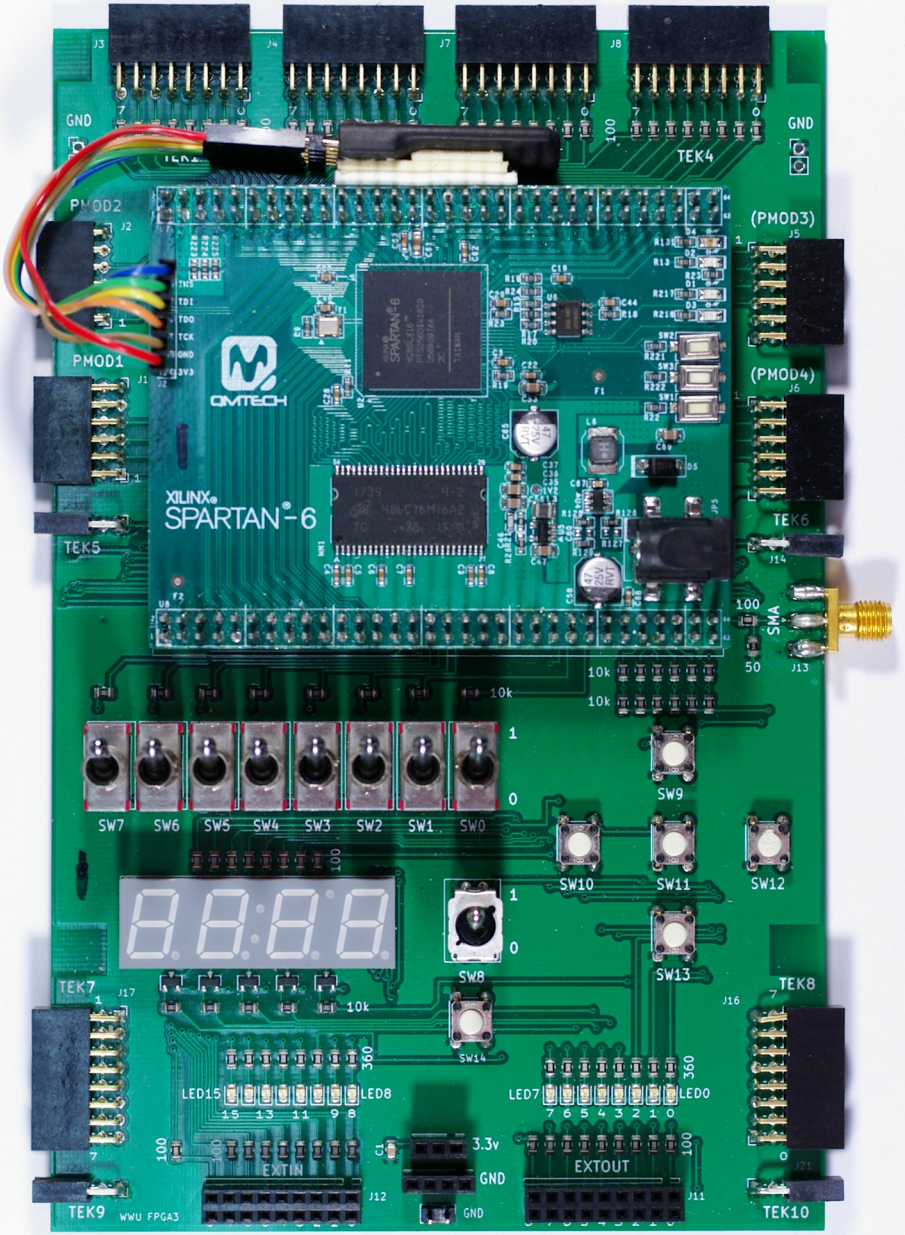
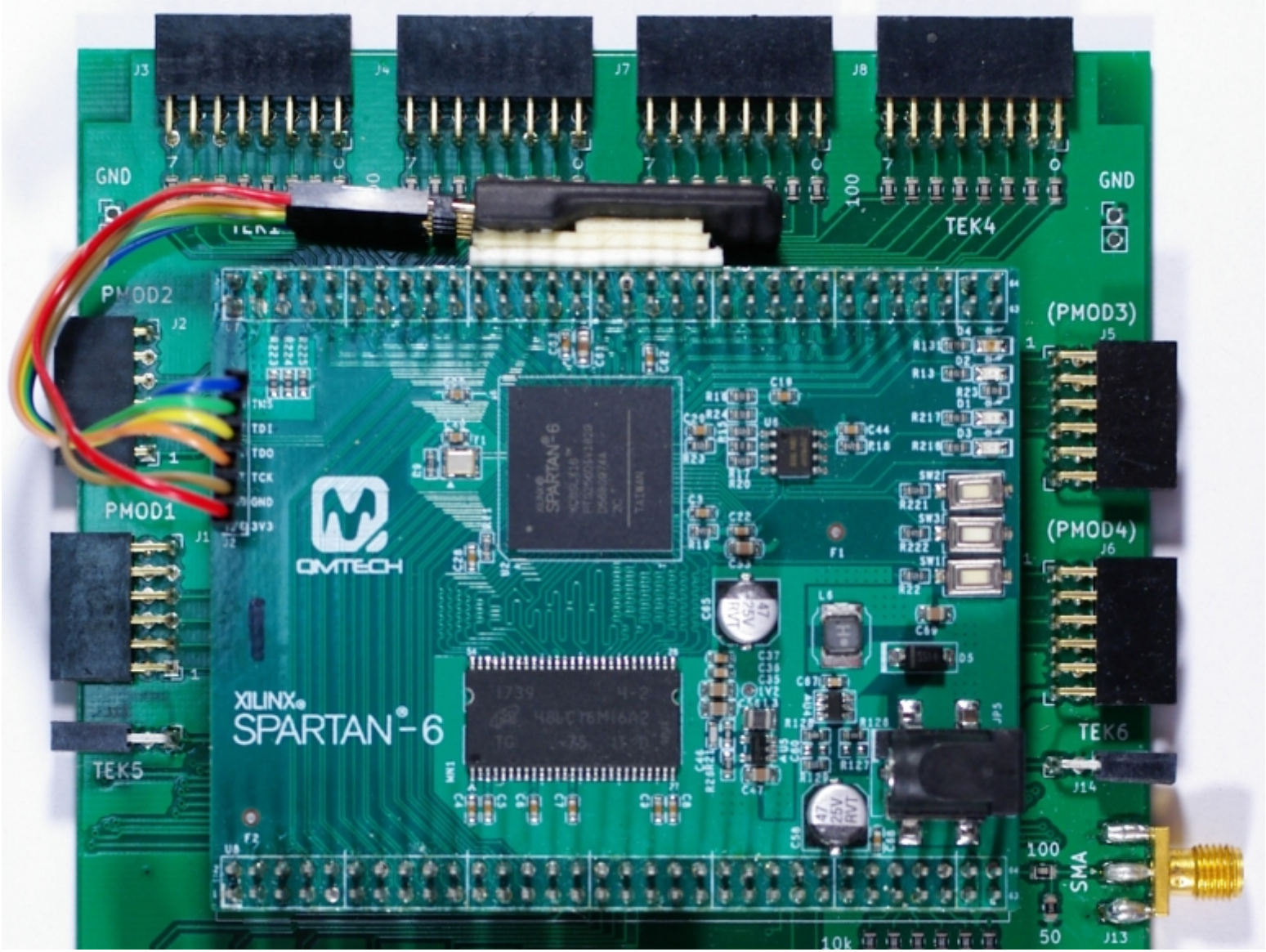
111
000
Z↓↑ if X


GND
TEK4
PMOD2
(PMOD3)
PMOD1
(PMOD4)
QMTECH
XILINX
SPARTAN-6
TEK5
TEK6
SMA
10k
SW7
SW6
SW5
SW4
SW3
SW2
SW1
SW0
SW9
SW10
SW11
SW12
SW8
SW13
SW14
TEK7
TEK8
LED15
LED8
LED7
LED0
EXTIN
EXTOUT
3.3v
GND
TEK9
WWU FPGA3
TEK10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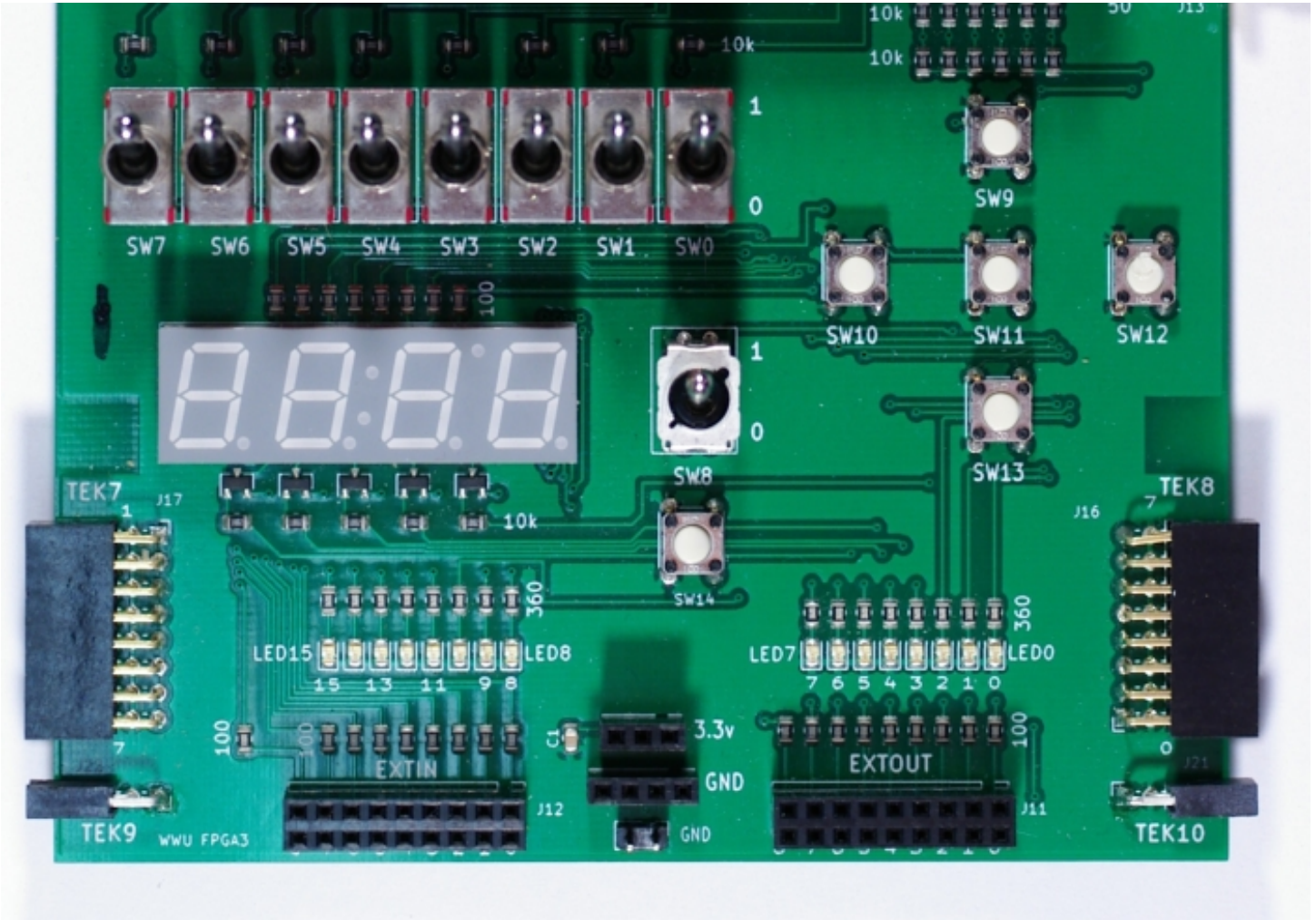
10k
10k
10k
1
0
SW7
SW6
SW5
SW4
SW3
SW2
SW1
SW0
SW9
SW10
SW11
SW12
SW13
SW8
SW14
100
10k
360
LED15
LED8
15 13 11 9 8
LED7
LED0
7 6 5 4 3 2 1 0
TEK7
J17
TEK8
J16
TEK9
TEK10
EXTIN
EXTOUT
J12
J11
C1
3.3v
GND
GND
WWU FPGA3