Lab Exercise #6

Objective

The objective of this lab is to continue learning VHDL by designing and implementing a circuit containing both combinational and sequential logic circuits.

References

On-line from the class webpage are manuals for the Xilinx software and hardware.

Design Flow

The general design flow we are using is described below.

- Initial design (block diagram in particular)
- Describe the design using VHDL
- Synthesize using Xilinx software
- Download to FPGA board using Impact
- Verify waveform with logic analyzer.or scope

Problem Statement

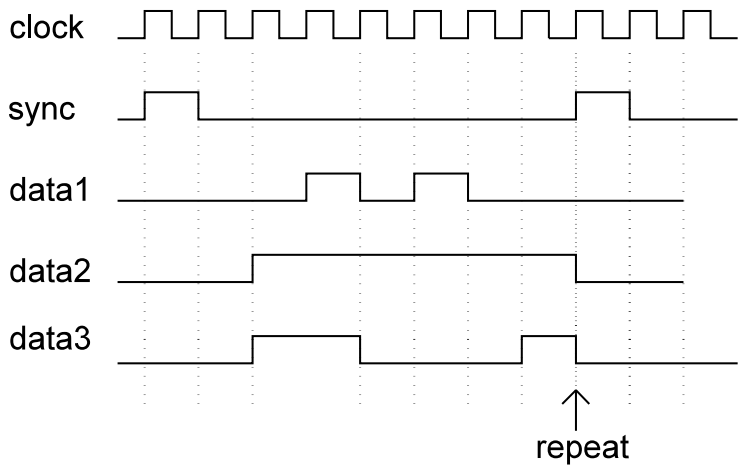
Design a logic circuit that will create the set of waveforms shown in figure1. The "clock" shown in figure 1 is a derived clock, not 50Mhz, with 50Khz rate. It should be able to start/stop waveform output using sw0. Sw0 should be an input to the first state of your state machine. If it is 0, then hold in the first state and don't generate the sync signal and don't transition to other states. If sw0 is a 1 then generate the sync signal in the first state and continue to transition through the complete state sequence.

The 50Mhz master clock, derived clock, and four waveform signals (sync, data1, data2, data3) are all to be routed to FPGA output pins (definition on the next page). Other signals at your discretion. This is to allow observation of the waveforms with an oscilloscope or logic analyzer.

Initial Design

Before writing any VHDL create a neatly drawn, fully documented, state diagram (pencil/paper or electronic tool) showing the circuit function needed. Normally a block diagram should be drawn, although for this lab there are few blocks needed When writing the VHDL description do use dividing lines and label the components of the circuit to allow easy identification of statements that relate to each component. You don't need to create separate entities/architectures for the parts used in this design. You can have one entity for the overall design and one architecture with multiple processes and assignment statements (with appropriate comments) that reflect the functional part of the circuit.

A clock generation VHDL description is on the class web page.



Lab 6 - figure 1

FPGA Pinout Definition

This definition assumes a WWU FPGA3 board with a Spartan6 FPGA.

Input Connections
Master clock (50Mhz)
sw0

Output Signal	Connections
Sync	Extout(0), TEK1(0)
Data1	Extout(1), TEK1(1)
Data2	Extout(2), TEK1(2)
Data3	Extout(3), TEK1(3)
Derived clock	Extout(4), TEK1(4)
Master clock (50Mhz)	Extout(7), TEK1(7), TEK5

To Turn In

Your design details. Should include a good quality block diagram, any design notes, VHDL listing. The block diagram can be hand drawn but should be drawn with a straight edge or template and neatly labeled.

A report is required from each person and consists of:

- a one page synopsis of what you did in lab, procedures followed, results, and problems if any.
- block diagram
- a copy of the VHDL definition
- statistics: number of slice F/Flops used, # of occupied slices, # of slices containing unrelated logic, number of bonded IOBs, the number of BUFGMUXs, and average fanout of non-clock nets (this information can be documented with a screen shot)