# Lab Exercise #3

## Objectives

- Gain further experience using state machines, counters, multiplexers, etc.
- Gain further experience with schematic driven design to reinforce an understanding of typical circuits that in future labs will be described with a hardware description language.

## References

Xilinx documents on the class web page.
Pinout for the WWU FPGA3 digital logic board (found on the class webpage)

## Problem Statement

Design a "stop watch" circuit that will measure time up to 99 seconds in hundredths of seconds and display the measured time in 4 decimal digits, two for seconds, two for hundredths. There will be two buttons used to operate the stop watch. Button one will be pressed to start time and pressed a second time to stop time. Button two will be used to reset time to zero once counting has stopped. Time is to be displayed in base 10 on a 7-segment display that has 4 digits plus a colon to denote separation between seconds and fractions of seconds. Use a state machine to monitor the buttons and assert control signals needed by the counters.

A stretch goal would be to have a third button that allows display of lap time, i.e. pressing the third button would freeze the current time on the display while allowing the counters to continue running and measuring the total elapsed time. Pressing this third button a second time would cause the display to revert to "running" time.

## Design Flow

The general design flow for today's lab is:

- Design a circuit per the problem statement.
  - Confirm understanding of the problem & partition the design into subsystems.
  - Create a block diagram
  - Create a fully documented state diagram.
  - Create logic functions for the next-state and output logic
  - From the Xilinx library, find components and understand their operation.
- Create a schematic for your design using the Xilinx schematic tool
- Synthesize an FPGA implementation (Place, route, and create a bit map file)
- Download bit map file to the FPGA board
- Verify correct operation (debug if needed)

Specific input/output resources to use:

sw12 will be the main button, i.e. the start/stop button
sw9 will be the reset switch
sw13 will be the lap button (if used)
display will be on the 7-segment display

The Xilinx library for schematic driven design contains D flip-flops, D latches, counters, many types of AND, OR, NAND, NOR, XOR gates with various numbers of inputs, 2:1 mux, 4:1 mux, 8:1 mux, 2:4 decoder, 3:8 decoder, RAM/ROM, etc.

**Suggestion to aid debugging**

Because you cannot connect a scope probe onto circuit nodes inside an FPGA, bring out signals that would be useful for debugging using the ExtOut signal lines where a scope can be connected. If signals change slowly enough connect signals to LEDs to observe them.

**A note about schematic drawing**

The schematic should appear centered on the schematic sheet. Parts should be evenly distributed across a sheet and not all scrunched up in one corner. Use multiple sheets if needed to make the schematic very readable. Signal names (nets) should be meaningful. A title block must appear on each sheet.

## To Turn In

- By next lab period, a short report containing:
  Abstract (which includes a statement about results), block diagram, schematic, summary statement commenting on any problems encountered, things learned, etc. If intellectual property (IP) created by someone else is used in the design give credit to the source (IP here would refer to a circuit or possibly the design of a state machine, etc.).