How to test the 8x16 display 11/11/20

On the class webpage there is a bit file that defines a circuit for dynamically testing the 8x16 LED display. The procedure to follow to load and use this circuit follows.

- Connect the 8x16 LED display to the extout port on the WWU FPGA board. 8 data lines plus power and ground are required. Refer to a diagram available on the class web page titled "8x16 LED display connection details (pdf)" found under the *Display hardware info* section of the web page.
- 2) Download the bit file from the class web page found in the *Display hardware info* section of the web page as Circuit to test 8x16 LED display. There are two versions:
 test_led_display_fpga3_sdram.bit
 pick the version that matches your board test_led_display_fpga3_ddr3.bit
- 3) You can download the bit file to your FPGA board without starting ISE by directly starting the Impact program. Or if you have ISE running you can start Impact in the usual way and when prompted for a configuration file navigate to where you saved the selected file.

To use the Impact program stand alone, i.e. starting it directly without starting ISE do this:

- 1) Download the "test_led_display_fpga3_xxxx.bit" file to an appropriate folder.
- 2) Start a terminal window and navigate to the folder where the bit file is located (use the cd command to navigate between directories and folders)
- 3) Enter impact (all lower case) and press return. The Impact program should start.
- 4) The Impact starting screen should appear:



5) A second smaller window will also be displayed:



Click No.

6) The New Project window will open:

	New iMPACT Project	- + x
I want to		
Ioad most recent project	pulse_gen_project.ipf	▼ <u>B</u> rowse
	Load most recent project file when	MPACT starts
C create a new project (.ipf)	default.ipf	Browse
<u></u>	<u>C</u> ancel	

Click Cancel.

- 7) In the main Impact window double click on Boundary Scan. The right hand part of the window will change with a boundary scan tab shown at the bottom.
- 8) In the right part of the window right click and this box should appear:

Add Xilinx Device	Ctrl+D	
Add <u>N</u> on-Xilinx Device	Ctrl+K	
Initialize Chain	Ctrl+I	
<u>C</u> able Auto Connect Cable <u>S</u> etup		
<u>O</u> utput File Type	+	

Click **Initialize Chain**. The programming cable should connect. Icons for the FPGA and memory should appear.

9) The remaining steps to load the configuration file and then download to the FPGA are the same as when starting Impact from ISE. If needed, refer to pages 8 tol1 in the document "Notes for schematic driven design (pdf)" which detail using Impact. That document is found under the heading *Notes and user information* on the class web page.