

ENGR433 - Digital Design
Fall 2020

			Textbook: RTL Hardware Design Using VHDL by Pong Chu			
Date		Topic			Reading	
M	Sept	14	Quiz (handout sent), Class intro, state machine operation		Handout	
W		16	Classical state machine design		Handout	
F		18	Introduction to Xilinx FPGAs		Handout	
M		21	State machine design with one-hot state encoding		Handout	
W		23	Design abstraction, synthesis, Intro to VHDL		1.1-6, 2.1	
F		25	VHDL by example		2.2-3	
M		28	VHDL language basics		3.1-4	
W		30	Data types and operators		3.5-6	
F	Oct	2	Concurrent signal assignment statements		4.1-3	
M		5	Selected signal assignment statements		4.4-6	
W		7	Sequential statements		5.1-4	
F		9	Sequential statements		5.4-5, 5.8	
M		12	Memory and sequential circuit design		8.1-4	
M		14	Counter basics		8.5	
F		16	Exam 1			
M		19	Finite state machines in VHDL		10.1-2, 10.5.2	
W		21	State machine timing, Moore vs Mealy outputs		10.3-4	
F		23	State assignment, output buffering, edge detection		10.5-7, 10.8.1	
M		26	Poor design practices and remedies		9.1	
W		28	Realization of VHDL operators		6.2-3	
F		30	Timing considerations, hazards		6.5	
M	Nov	2	Input synchronization; Meta-stability		16.4-5	
W		4	Electrical design of logic circuits		Handout	
F		6	More FPGA details (electrical details)		Handout	
M		9	Exam 2			
W		11	Electrical design, more details		Handout	
F		13	Resource sharing in logic circuits		7.2-3	
M		16	Testing with simulation - test benches		Handout	
W		18	Wrap up			
F		20	Review day - no class			

Sunday November 22 - Final Exam time 10am, required class meeting