Digilent 2E FPGA board with DIO1 I/O board attached to connectors A\&B or E\&F FPGA Pin numbers

| Function | FPGA pin\# |  |
| :---: | :---: | :---: |
| SW1 | 16 | Slide switches |
| SW2 | 18 |  |
| SW3 | 21 |  |
| SW4 | 23 |  |
| SW5 | 27 |  |
| SW6 | 30 |  |
| SW7 | 33 |  |
| SW8 | 35 |  |
| BTN1 | 40 | Push buttons (momentary). Asserted high when pressed. |
| BTN2 | 41 |  |
| BTN3 | 42 |  |
| BTN4 | 43 |  |
| BTN5 | 64 |  |
| LD1 | 44 | LEDs, individual. Asserted high. |
| LD2 | 46 |  |
| LD3 | 48 |  |
| LD4 | 55 |  |
| LD5 | 57 |  |
| LD6 | 59 |  |
| LD7 | 61 |  |
| LD8 | 63 |  |
| CA | 17 | 7-segment display (individual segments, cathodes). Asserted low. |
| CB | 20 |  |
| CC | 22 |  |
| CD | 24 |  |
| CE | 29 |  |
| CF | 31 |  |
| CG | 34 |  |
| DP | 36 | Decimal point of the 7-segment display. Asserted low. |
| A1 | 45 | Anodes for the 4 display digits. Asserted high. |
| A2 | 47 | (tie unused anodes low) |
| A3 | 49 |  |
| A4 | 56 |  |

Note: Only one digit of the four digit 7-segment display can be used at a time. Assert one of the Anode signals (A1 to A4) at a time corresponding to the digit that should be on. If a four digit number is to be displayed, the Anode signals must be turned on sequentially and the data driving the cathodes multiplexed to be the data appropriate for the digit that is selected.

| Function | FPGA pin\# |  |
| :--- | :---: | :--- |
| keybd clock (PS2C) | 187 |  |
| keybd data (PS2D) | 189 |  |
|  |  |  |
| vga-blue | 188 |  |
| vga-green | 191 |  |
| vga-red | 193 |  |
| HSync | 192 |  |
| VSync | 194 |  |
|  |  |  |
| 50 Mhz clock | 80 | Global clock 0 |
| BTN1 on fpga bd | 77 | Global clock 1 |
| B12 ext clock in | 182 | Global clock 2 |
| B11 ext clock in | 185 | Global clock 3 |

