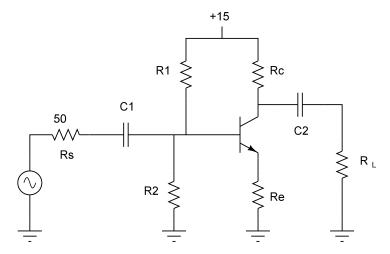
ENGR-356 Lab # 8 Common-Emitter Amplifier

Goals

The principle goal is to investigate and to understand the biasing and large signal operation of a common-emitter amplifier.

Design

Using the circuit topology shown in figure 1, complete a design that has the following performance: Rin > 20k, voltage gain (maximize, but at least > 5), low distortion.



The general approach is to find the DC Q point while keeping in mind the expressions for gain. Recall that small signal gain will depend on Beta, Re, Rout, Rload, re. Attempt to achieve the stated gain without bypassing Re. Likely you will find that the value of Rload will have a significant effect on gain. You might try an initial design without Rload and then add it.

Measurements should include:

Gain, range of frequencies where the output drops to no less than .707 of the maximum given a constant level input voltage, the maximum p-p output voltage without significant distortion.

Documentation

Take careful notes in your lab notebook.

Lab Report

The lab report will be one page on which you document the following:

- Component values for R1, R2, Rc, Re, C1, C2 in your breadboarded circuit.
- Calculated Rin and Voltage gain
- Measured voltage gain at 10Khz
- Measured maximum p-p output without significant distortion
- Measured frequency range (between the -3db points)
- Observations about the lab (challenges, what worked, what didn't, etc).