Electrical Design of Digital Logic Circuits

This note assumes that the reader understands digital logic circuits from a logic, i.e. boolean algebra, point of view. For example, logic functions such as AND, OR, NOT, NAND, NOR, XOR, EQV are known and understood.

Traditionally the power source for digital logic devices (called Vcc or Vdd) was 5 volts. Then 3.3V became standard for many devices including the input/output circuits of modern microprocessors and microcontrollers. This reduction in voltage was needed because transistor size and associated dielectric thickness in MOSFET (Metal Oxide Semiconductor Field Effect Transistors) decreased thereby decreasing the breakdown voltage of internal insulation layers. A decrease in voltage also decreased power consumption and thus improved battery life for battery operated devices and reduced heat generation since according to Ohms law $P = E^2/R$. More recently voltage for the core circuits of microprocessors and microcontrollers has dropped further, as low as 1.0 volts, to reduce power consumption. For the remainder of this document a 3.3V power supply voltage will be assumed. (there are still many circuits, such as USB, that run at 5 volts)

When connecting logic devices together and particularly when connecting peripheral circuits to microprocessors or microcontrollers, the voltage and current characteristics of the components being interconnected need to be carefully checked for correctness.

DC Input and Output Voltage Calculations - Noise Margin

A digital circuit must have what is called a noise margin in both its logic high and logic low conditions. Figure 1 below details the definition of Noise Margin High (NMH) and Noise Margin Low (NML) which is the difference between the output voltage of the logic circuit that is creating a signal and the required input voltage of a logic circuit receiving that signal. The larger the noise margin the more tolerant the circuit is to any noise voltage that might get added to the desired signal. As long as the noise voltage magnitude is less than the noise margin it will not affect operation.

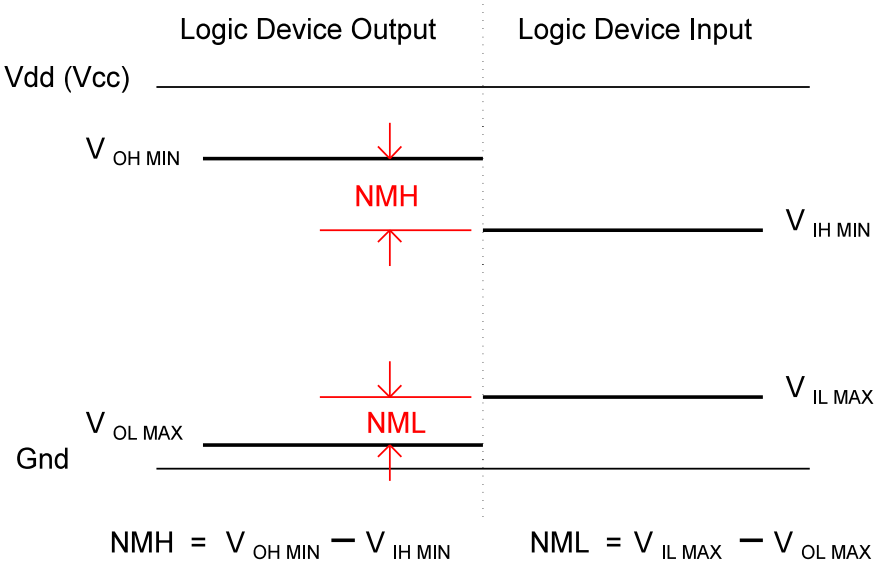

Figure 1 - Noise margin definition

Figure 2 illustrates a possible circuit and the evaluation of noise margin..

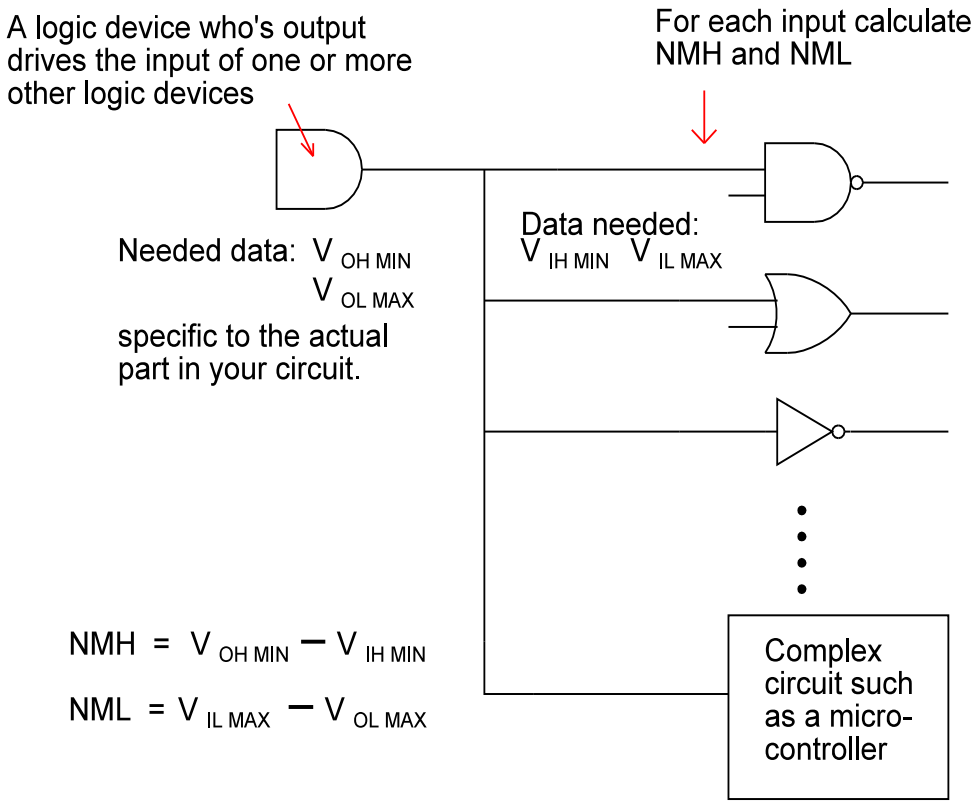

Figure 2 - Example circuit for noise margin evaluation.

Input and Output Current Evaluation (DC)

The currents that flow between a component that is creating a logic signal and the circuit that is receiving that signal must also be analyzed when designing digital systems. For logic circuits, when the output of a logic device is at a high logic output current flows out of the device and we say the device is sourcing current, i.e. current is flowing from the Vdd (or Vss) supply terminal to the output. When at a logic low, current flows into the device and we say the device is sinking current, i.e. the current is flowing to ground.

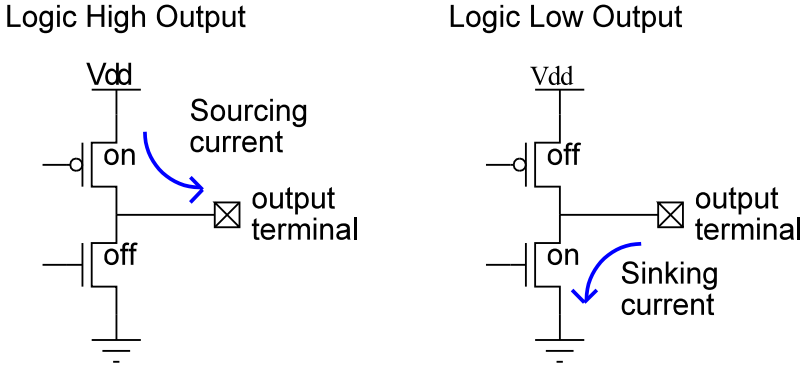

Figure 3 - Typical output circuit and current direction

Figures 4 and 5 on the next page illustrate analyzing current requirements for proper circuit operation.

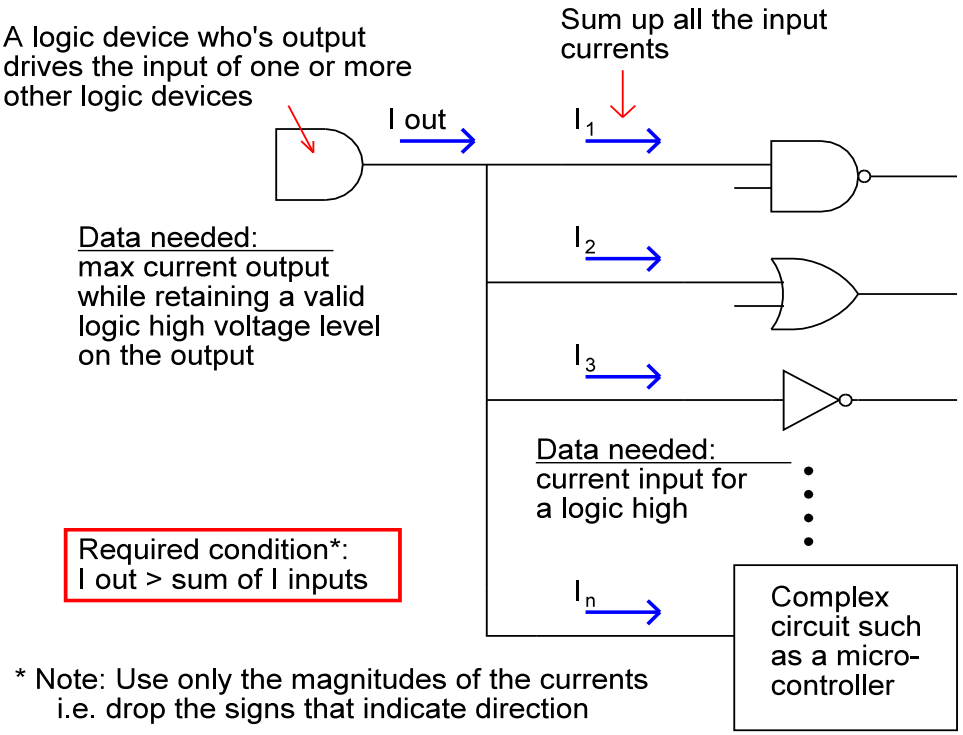

Figure 4 - Current calculation for logic high

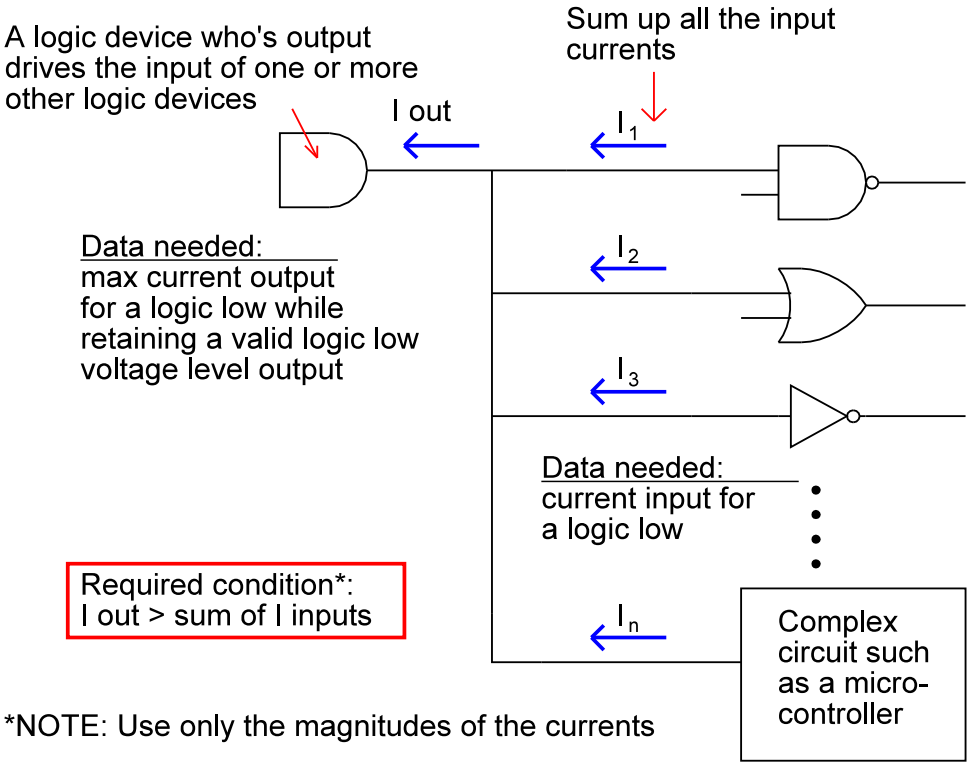

Figure 5 - Current calculation for logic low

Figures 4 and 5 show currents that flow in or out of a logic device, i.e. logic gate. In data sheets, by standard convention, the sign shown on a current indicates direction of current flow. Current flowing in is positive (+) and current flowing out is negative (-) for both the outputs and inputs of logic gates.

Logic Switching Characteristics (sometimes labeled AC characteristics)

The current calculation in figures 4 and 5 are DC calculations. When logic outputs are switching from one logic state to the other, the time it takes to switch and the corresponding rate of voltage change depends on total load capacitance and the available output current when going low-to-high or the capacity to sink current when going high-to-low.

Most modern logic circuit designs incorporate integrated circuits constructed using CMOS technology. While these circuits do have DC current requirements in both logic high and low states, the input capacitance of a gate is more significant in determining switching times. Also note that wiring between gates, such as traces on a circuit board, contribute to the total capacitance on the output of a driving circuit and hence the switching time. Switching time is denoted as signal rise-time or signal fall-time depending on direction of change.

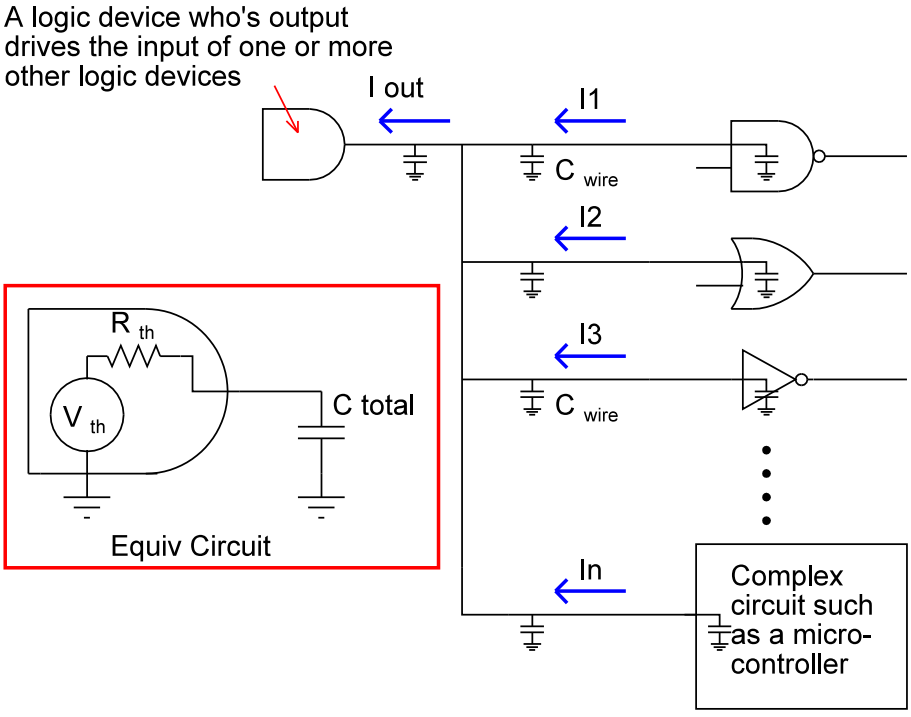

Figure 6 - Circuit capacitances and driving circuit

Consider a logic level transition from high to low voltage. A logic gate driving one or more other circuits can be modeled as a Thevenin voltage source with a Thevenin resistance and the circuits being driven as a capacitance that is the sum of the input capacitances of the load circuits plus wiring capacitance between driving device and all the loads. A simplified circuit model can then be derived as shown in figure 6. Note that for a high to low transition R_{th} is an N type transistor as shown in figure 3 and as such it is not a simple resistance, i.e. as a transistor

switches, its equivalent output resistance is not constant but changes as the transistor transitions through its modes of operation. Thus the wave shape is not a simple exponential as would be the case with a pure resistance and capacitance. However, a simple resistor-capacitor model is useful for developing an understanding of circuit behavior and estimating performance (circuit simulators such as SPICE can be used to better predict circuit waveshape and timing if transistor parameters, specific to the technology used to create the logic gate, are known).

In short, for a particular logic gate driving other gates, the larger the load capacitance the longer it takes to transition from one logic level to the other.

Further information on output loading of a logic gate

As discussed above, the Vout maximum for logic low and the Vout minimum for logic high are needed to calculate noise margin. These values can be found in the data sheet for a particular component. Below is a table from the Texas Instruments data sheet for the SN74LS00 (the 54LS00 is specified over a wider temperature range).

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			SN54LS00			SN74LS00			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = –18 mA				–1.5			–1.5	V
V_{OH}	V_{CC} = MIN,	V_{IL} = MAX,	I_{OH} = –0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8mA					0.35	0.5	
I_I	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7V				20			20	µA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V				–0.4			–0.4	mA
I_{OS}§	V_{CC} = MAX			–20		–100	–20		–100	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			0.8	1.6		0.8	1.6	mA
I_{CCL}	V_{CC} = MAX,	V_I = 4.5 V			2.4	4.4		2.4	4.4	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

Figure 7 - SN74LS00 NAND gate electrical specifications

Note that for V_{OH} the test conditions state the current I_{OH} is -0.4mA where the minus sign indicates this current is flowing out of the gate. The typical V_{OH} is 3.4 volts but the minimum is 2.7 volts. Use the 2.7 value in noise margin calculations. And for current calculations use the 0.4 mA as the largest allowed output current.

V_{OL} is specified at two different output currents, 4mA and 8mA, with corresponding maximum voltages of 0.4 or 0.5 volts respectively. Again, for purposes of determining maximum allowed loading and resulting noise margin use one of these currents with its respective output voltage.

The output voltage of a gate takes on a range of values as a function of current. In the high logic state an output with light load will have a higher voltage than an output with a heavy load. Figure 8 shows the schematic for a SN7400 gate (the SN74LS00 uses a similar topology with some additional parts and Shockley transistors). It should be apparent from the schematic that with a 5 volt power source the output voltage will never be as high as 5 volts due to the required base-emitter voltage of the output transistor plus forward drop across the diode. Graphs of voltage as a function of current can be found in the semiconductors flyers and reference books.

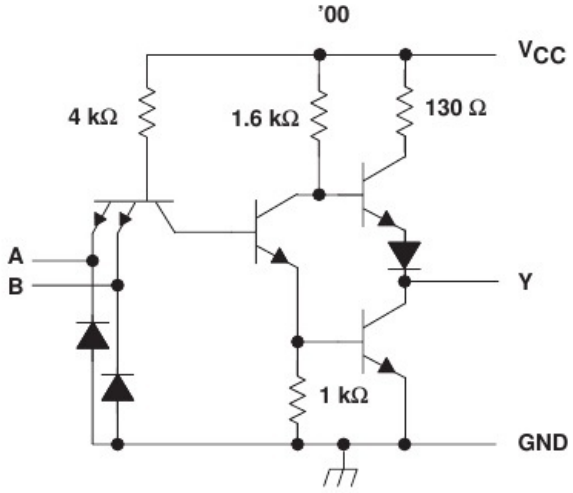

Figure 8 - Schematic of a SN7400 NAND gate

Below are ON Semiconductor company graphs for 74LS00 output voltage versus current.

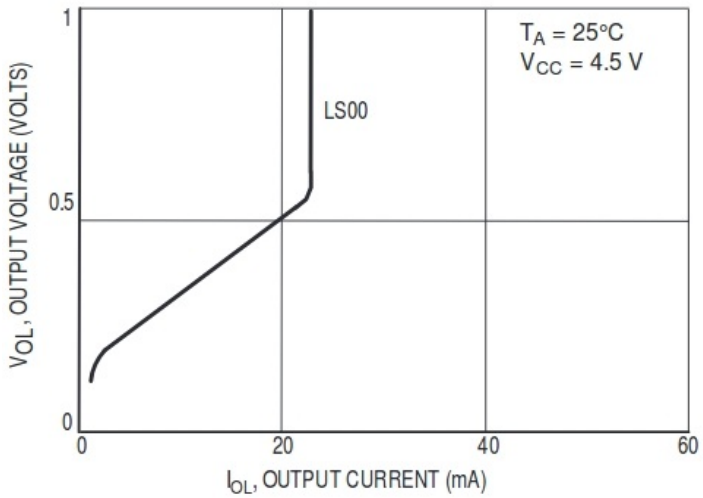

Figure 9 - 74LS00 logic zero output

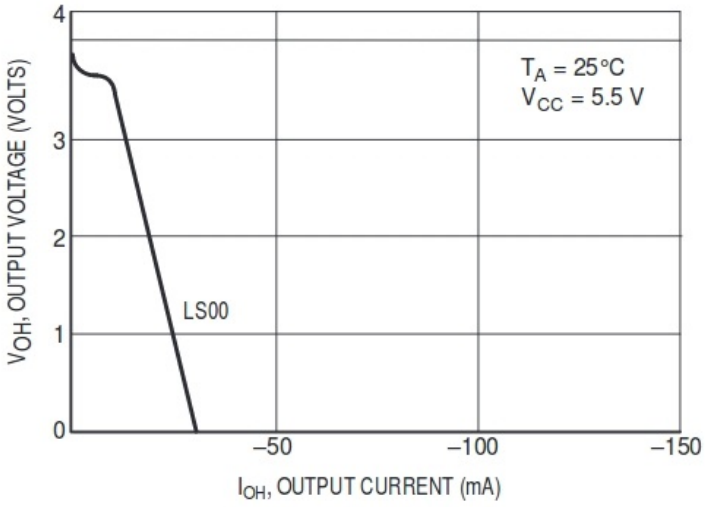

Figure 10 - 74LS00 logic one output

by Larry Aamodt rev3