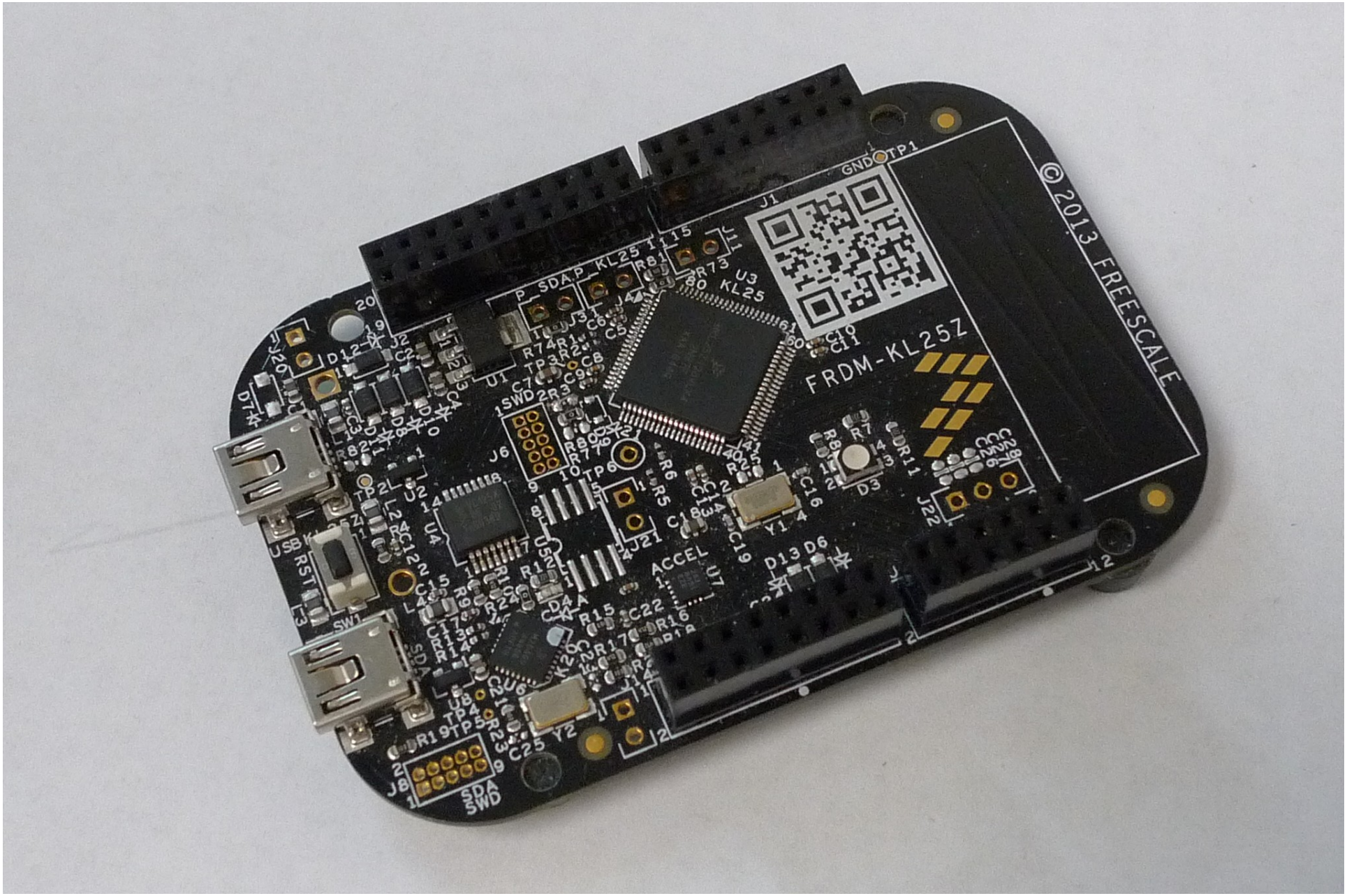
A First Look at Microcontroller Configuration

Kinetis L-Series
KL25Z128VLK4


FRDM-KL25Z
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U3
KL25
U1
U2
U4
U5
U6
U7
ACCEL
J1
J2
J3
J4
J6
J8
J11
J21
J22
SW1
RST
USB
SDA
SWD
GND
TP1
Y1
Y2
D3
D4
D6
D12
D13

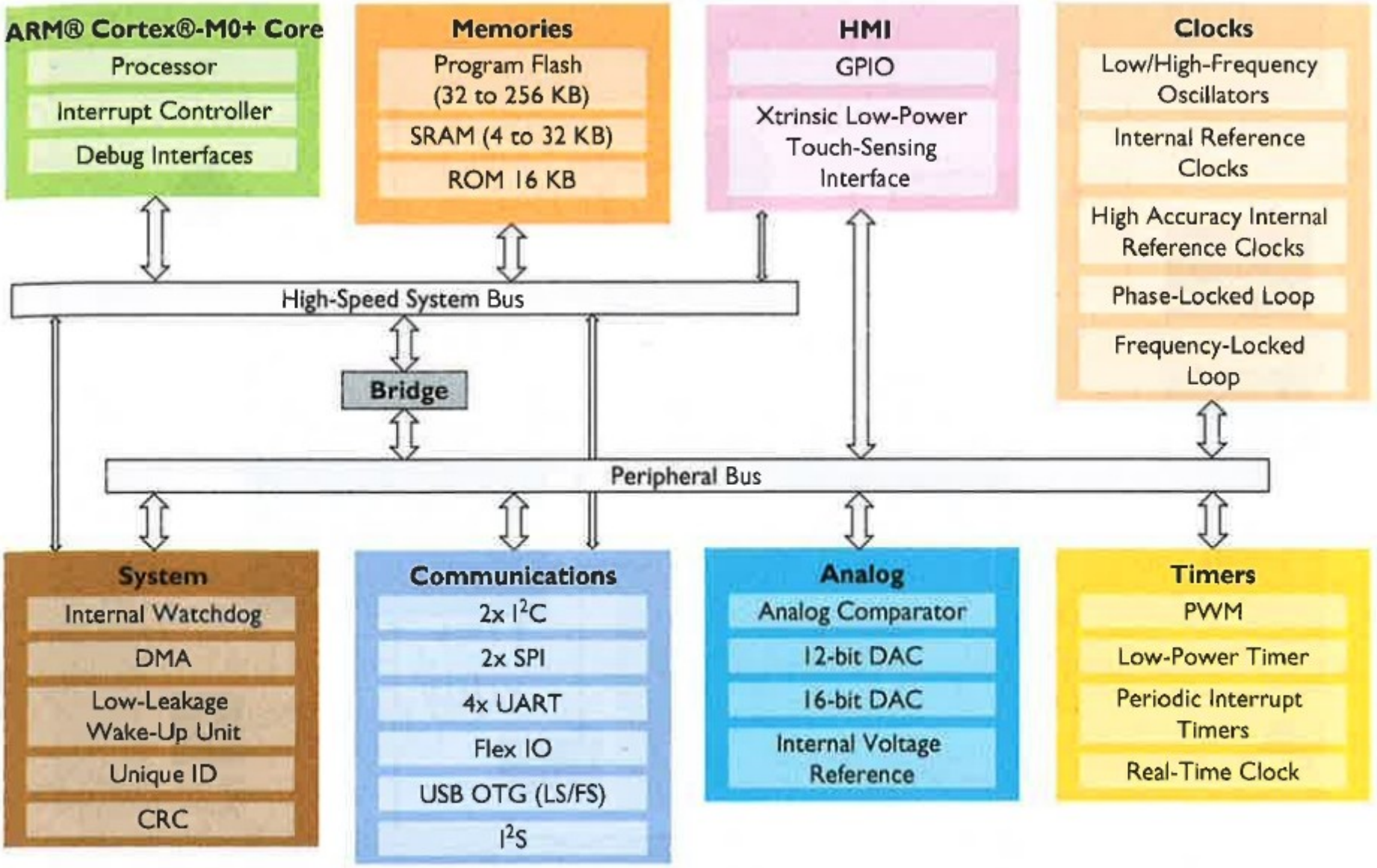


Figure 1.17 NXP Kinetis KL25Z family microcontroller (MCU).

NXP Processor and FRDM-KL25Z Development Board Documentation

- [1] NXP Kinetis KL25 processor sub-family data sheet (pdf)
- [2] NXP Kinetis KL25 processor sub-family reference manual (pdf)
- [3] FRDM-KL25Z development board schematics (pdf)
- [4] FRDM-KL25Z development board user manual (pdf)
- [5] Setting up Keil software for a FRDM-KL25Z development board (pdf)
- [6] Header file MKL25Z4.h (.h)

Freescale Semiconductor, Inc.
Data Sheet: Technical Data

Document Number: KL25P80M48SF0
Rev 5 08/2014

Kinetis KL25 Sub-Family

48 MHz Cortex-M0+ Based Microcontroller with USB

MKL25ZxxVFM4
MKL25ZxxVFT4
MKL25ZxxVLH4
MKL25ZxxVLK4

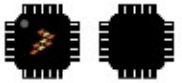
Designed with efficiency in mind. Compatible with all other Kinetis L families as well as Kinetis K2x family. General purpose MCU with USB 2.0, featuring market leading ultra low-power to provide developers an appropriate entry-level 32-bit solution.

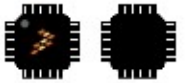
This product offers:

- Run power consumption down to 47 µA/MHz in very low power run mode
- Static power consumption down to 2 µA with full state retention and 4 µs wakeup
- Ultra-efficient Cortex-M0+ processor running up to 48 MHz with industry leading throughput
- Memory option is up to 128 KB flash and 16 KB RAM
- Energy-saving architecture is optimized for low power with 90 nm TFS technology, clock and power gating techniques, and zero wait state flash memory controller


32-pin QFN (FM)
5 x 5 x 1 Pitch 0.5 mm


48-pin QFN (FT)
7 x 7 x 1 Pitch 0.5 mm


64-pin LQFP (LH)
10 x 10 x 1.4 Pitch 0.5 mm


80-pin LQFP (LK)
12 x 12 x 1.4 Pitch 0.5 mm

Performance

- 48 MHz ARM® Cortex®-M0+ core

Memories and memory interfaces

- Up to 128 KB program flash memory
- Up to 16 KB SRAM

Human-machine interface

- Low-power hardware touch sensor interface (TSI)
- Up to 66 general-purpose input/output (GPIO)

Communication interfaces

- USB full-/low-speed On-the-Go controller with on-chip transceiver and 5 V to 3.3 V regulator

[1]

5 Pinout

5.1 KL25 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

80 LQFP	64 LQFP	48 QFN	32 QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1	1	—	1	PTE0	DISABLED		PTE0		UART1_TX	RTC_ CLKOUT	CMP0_OUT	I2C1_SDA	
2	2	—	—	PTE1	DISABLED		PTE1	SPI1_MOSI	UART1_RX		SPI1_MISO	I2C1_SCL	
3	—	—	—	PTE2	DISABLED		PTE2	SPI1_SCK					
4	—	—	—	PTE3	DISABLED		PTE3	SPI1_MISO			SPI1_MOSI		
5	—	—	—	PTE4	DISABLED		PTE4	SPI1_PCS0					
6	—	—	—	PTE5	DISABLED		PTE5						
7	3	1	—	VDD	VDD	VDD							
8	4	2	2	VSS	VSS	VSS							
9	5	3	3	USB0_DP	USB0_DP	USB0_DP							
10	6	4	4	USB0_DM	USB0_DM	USB0_DM							

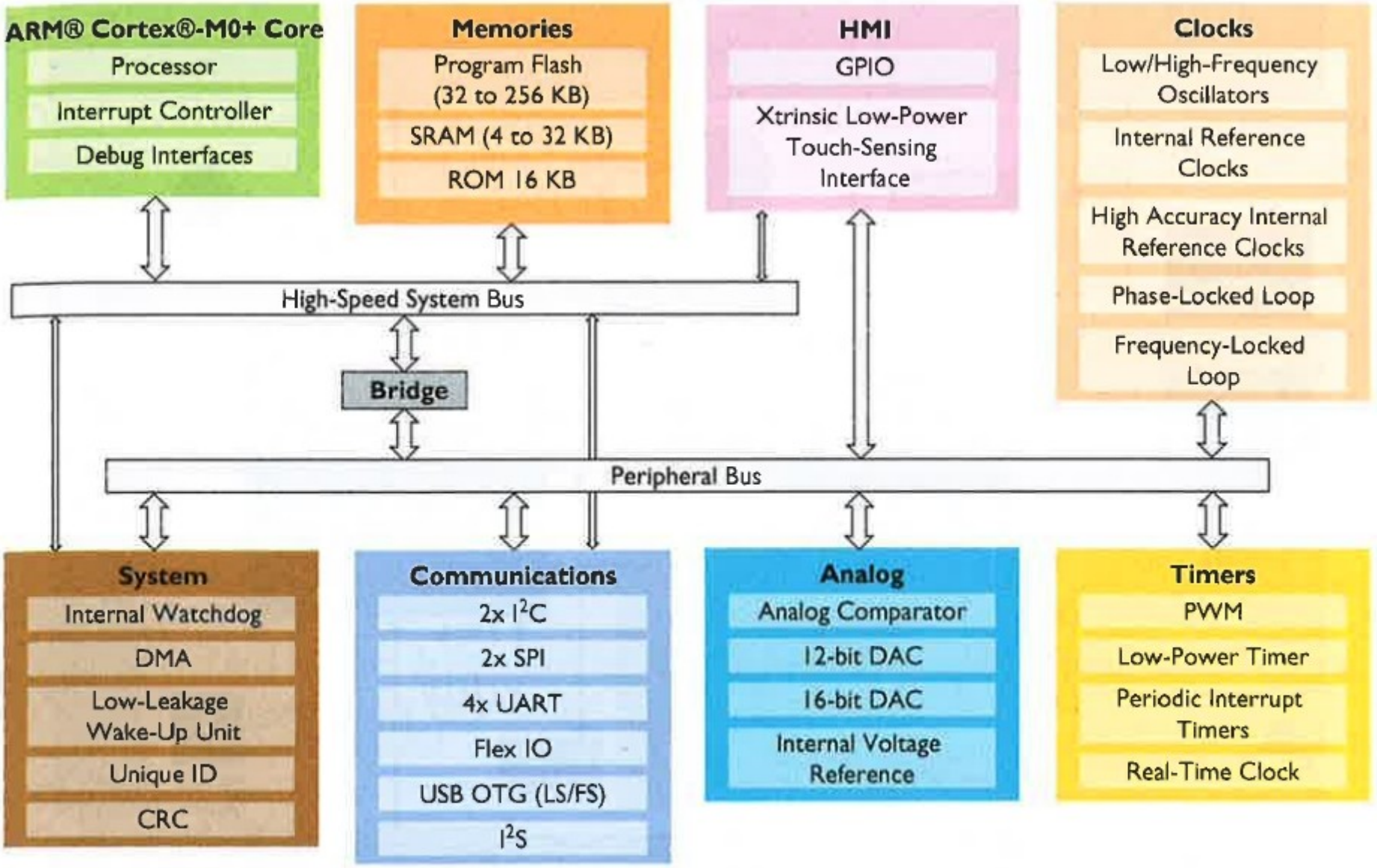


Figure 1.17 NXP Kinetis KL25Z family microcontroller (MCU).

Some of the circuits that need Input/Output pins

- A/D converter
- D/A converter
- UART (serial I/O)
- I2C
- USB
- SPI
- Input to start/stop a timer
- Pulse width modulation output from timer
- External clock input to timer
- Clock output – copy of the system clock
- General Purpose Input Output – GPIO
- and others

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- General Purpose Input Output – GPIO
- and others

How do all these functions relate to the physical pins on the chip?

First, there are five I/O ports defined in this microcontroller

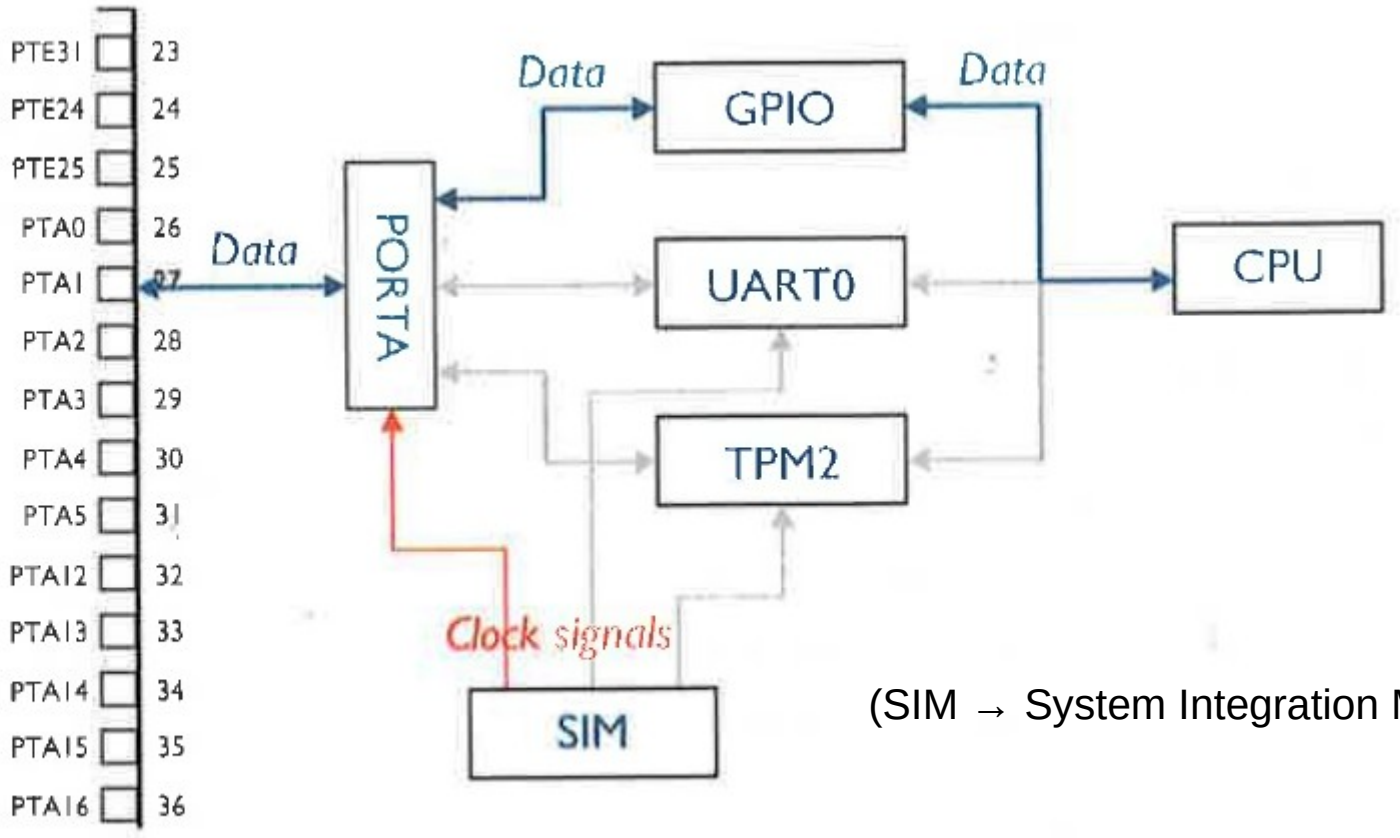
PortA
PortB
PortC
PortD
PortE

Each with up to 32 bits

Which means in theory there could be up to
32 x 5 = 160 pins for I/O on the chip

But, not all are used. Limited to available physical pins

5 I/O ports: A, B, C, D, E each with selected pin numbers between 0 and 31



(SIM → System Integration Module)

Figure 2.6 An overview of hardware between pin PTA1 and the CPU.

GPIO

Pinout

80 LQFP	64 LQFP	48 QFN	32 QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
44	36	28	21	PTB1	ADC0_SE9/ TSI0_CH6	ADC0_SE9/ TSI0_CH6	PTB1	I2C0_SDA	TPM1_CH1				
45	37	29	—	PTB2	ADC0_SE12/ TSI0_CH7	ADC0_SE12/ TSI0_CH7	PTB2	I2C0_SCL	TPM2_CH0				
46	38	30	—	PTB3	ADC0_SE13/ TSI0_CH8	ADC0_SE13/ TSI0_CH8	PTB3	I2C0_SDA	TPM2_CH1				
47	—	—	—	PTB8	DISABLED		PTB8		EXTRG_IN				
48	—	—	—	PTB9	DISABLED		PTB9						
49	—	—	—	PTB10	DISABLED		PTB10	SPI1_PCS0					
50	—	—	—	PTB11	DISABLED		PTB11	SPI1_SCK					
51	39	31	—	PTB16	TSI0_CH9	TSI0_CH9	PTB16	SPI1_MOSI	UART0_RX	TPM_ CLKIN0	SPI1_MISO		
52	40	32	—	PTB17	TSI0_CH10	TSI0_CH10	PTB17	SPI1_MISO	UART0_TX	TPM_ CLKIN1	SPI1_MOSI		
53	41	—	—	PTB18	TSI0_CH11	TSI0_CH11	PTB18		TPM2_CH0				
54	42	—	—	PTB19	TSI0_CH12	TSI0_CH12	PTB19		TPM2_CH1				
55	43	33	—	PTC0	ADC0_SE14/ TSI0_CH13	ADC0_SE14/ TSI0_CH13	PTC0		EXTRG_IN		CMP0_OUT		
56	44	34	22	PTC1/ LLWU_P6/ RTC_CLKIN	ADC0_SE15/ TSI0_CH14	ADC0_SE15/ TSI0_CH14	PTC1/ LLWU_P6/ RTC_CLKIN	I2C1_SCL		TPM0_CH0			

Also found in the family data sheet is electrical and timing info.
for example, electrical:

1.4 Voltage and current operating ratings

Table 4. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	120	mA
V_{IO}	IO pin input voltage	–0.3	V_{DD} + 0.3	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
V_{USB_DP}	USB_DP input voltage	–0.3	3.63	V
V_{USB_DM}	USB_DM input voltage	–0.3	3.63	V
V_{REGIN}	USB regulator input	–0.3	6.0	V

(pg 6 of data sheet)

2.2.1 Voltage and current operating requirements

Table 5. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	—
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	—
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	—
V_{IH}	Input high voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 0.7 × V_{DD} 0.75 × V_{DD}	 — —	 V V	—
V_{IL}	Input low voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 — —	 0.35 × V_{DD} 0.3 × V_{DD}	 V V	—
V_{HYS}	Input hysteresis	0.06 × V_{DD}	—	V	—
I_{ICIO}	IO pin negative DC injection current—single pin • V_{IN} < V_{SS}–0.3V	–3	—	mA	1
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins • Negative current injection	 –25	 —	 mA	—
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	2
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	—

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

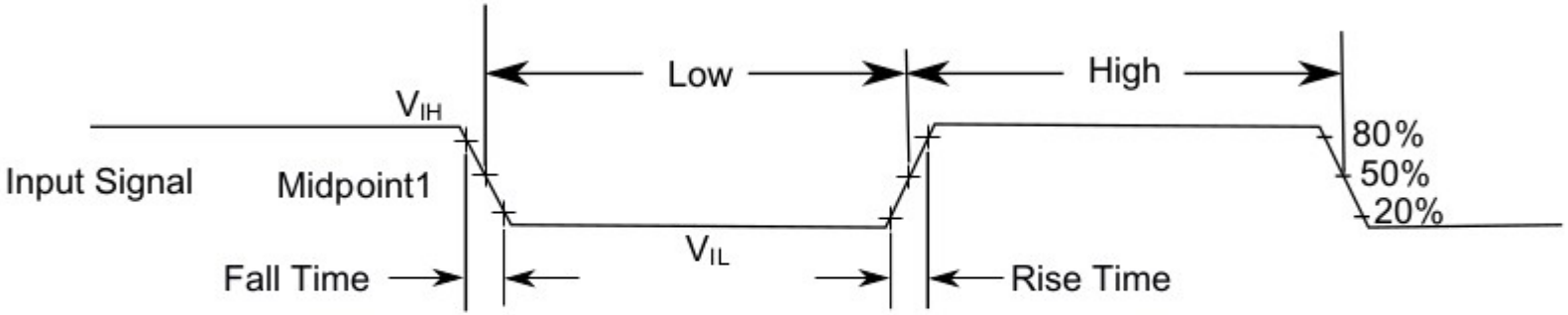


Figure 2. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume the output pins have the following characteristics.

- C_L=30 pF loads
- Slew rate disabled
- Normal drive strength

2.3.1 Device clock specifications

Table 13. Device clock specifications

Symbol	Description	Min.	Max.	Unit
Normal run mode				
f_{SYS}	System and core clock	—	48	MHz
f_{BUS}	Bus clock	—	24	MHz
f_{FLASH}	Flash clock	—	24	MHz
f_{SYS_USB}	System and core clock when Full Speed USB in operation	20	—	MHz
f_{LPTMR}	LPTMR clock	—	24	MHz
VLPR and VLPS modes[1]				
f_{SYS}	System and core clock	—	4	MHz
f_{BUS}	Bus clock	—	1	MHz
f_{FLASH}	Flash clock	—	1	MHz
f_{LPTMR}	LPTMR clock[2]	—	24	MHz

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KL25 Sub-Family Reference Manual

Supports: MKL25Z32VFM4, MKL25Z64VFM4, MKL25Z128VFM4,
MKL25Z32VFT4, MKL25Z64VFT4, MKL25Z128VFT4,
MKL25Z32VLH4, MKL25Z64VLH4, MKL25Z128VLH4,
MKL25Z32VLK4, MKL25Z64VLK4, and MKL25Z128VLK4

Document Number: KL25P80M48SF0RM
Rev. 3, September 2012

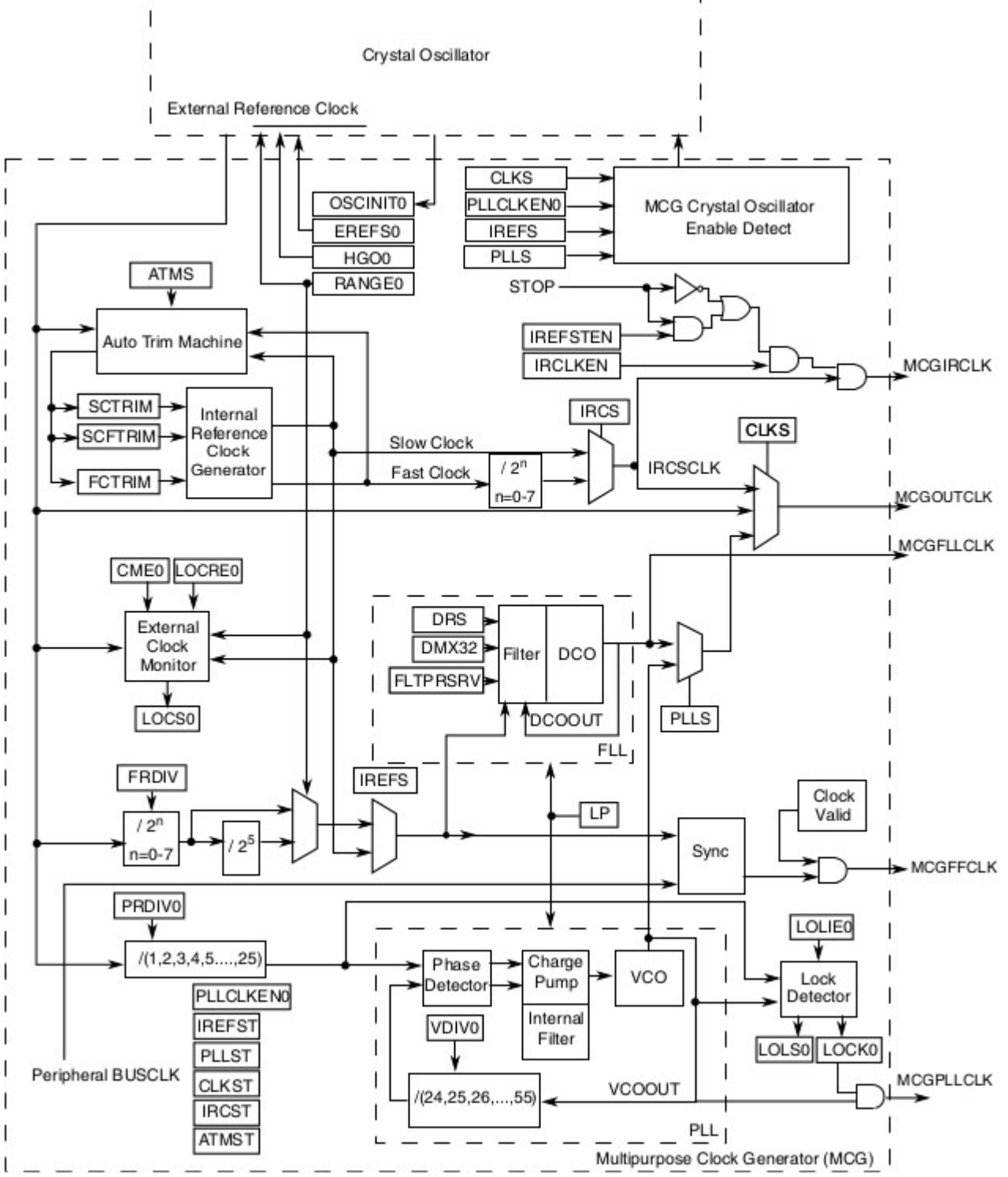

Figure 24-1. Multipurpose Clock Generator (MCG) block diagram

SIM memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4004_7000	System Options Register 1 (SIM_SOPT1)	32	R/W	See section	12.2.1/183
4004_7004	SOPT1 Configuration Register (SIM_SOPT1CFG)	32	R/W	0000_0000h	12.2.2/184
4004_8004	System Options Register 2 (SIM_SOPT2)	32	R/W	0000_0000h	12.2.3/185
4004_800C	System Options Register 4 (SIM_SOPT4)	32	R/W	0000_0000h	12.2.4/187
4004_8010	System Options Register 5 (SIM_SOPT5)	32	R/W	0000_0000h	12.2.5/189
4004_8018	System Options Register 7 (SIM_SOPT7)	32	R/W	0000_0000h	12.2.6/190
4004_8024	System Device Identification Register (SIM_SDID)	32	R	Undefined	12.2.7/192
4004_8034	System Clock Gating Control Register 4 (SIM_SCGC4)	32	R/W	F000_0030h	12.2.8/193
4004_8038	System Clock Gating Control Register 5 (SIM_SCGC5)	32	R/W	0000_0180h	12.2.9/195
4004_803C	System Clock Gating Control Register 6 (SIM_SCGC6)	32	R/W	0000_0001h	12.2.10/197
4004_8040	System Clock Gating Control Register 7 (SIM_SCGC7)	32	R/W	0000_0100h	12.2.11/199

Figure 2.4 A portion of registers for the System Integration Module (SIM) peripheral [1, p. 182].

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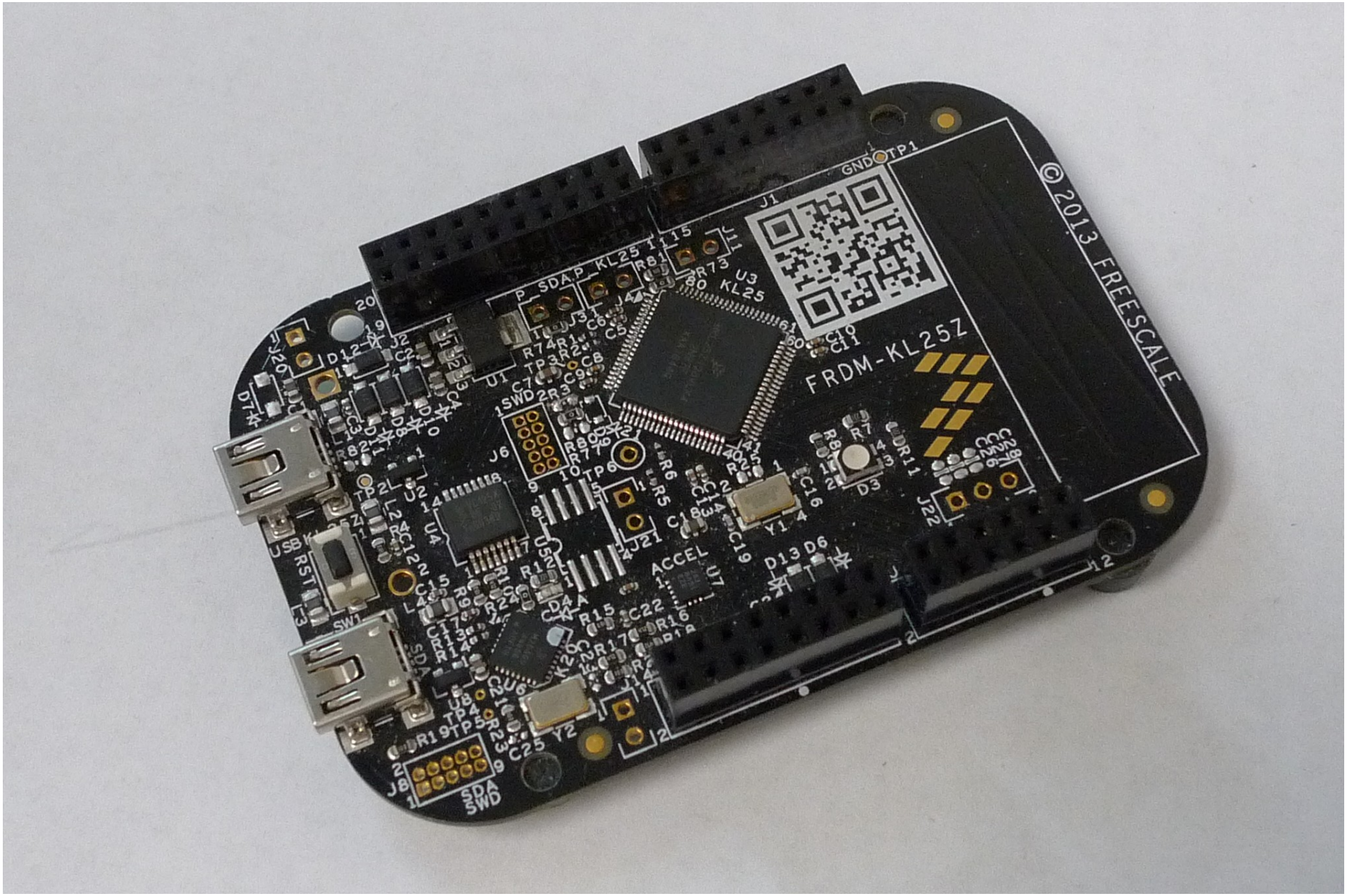
FRDM-KL25Z
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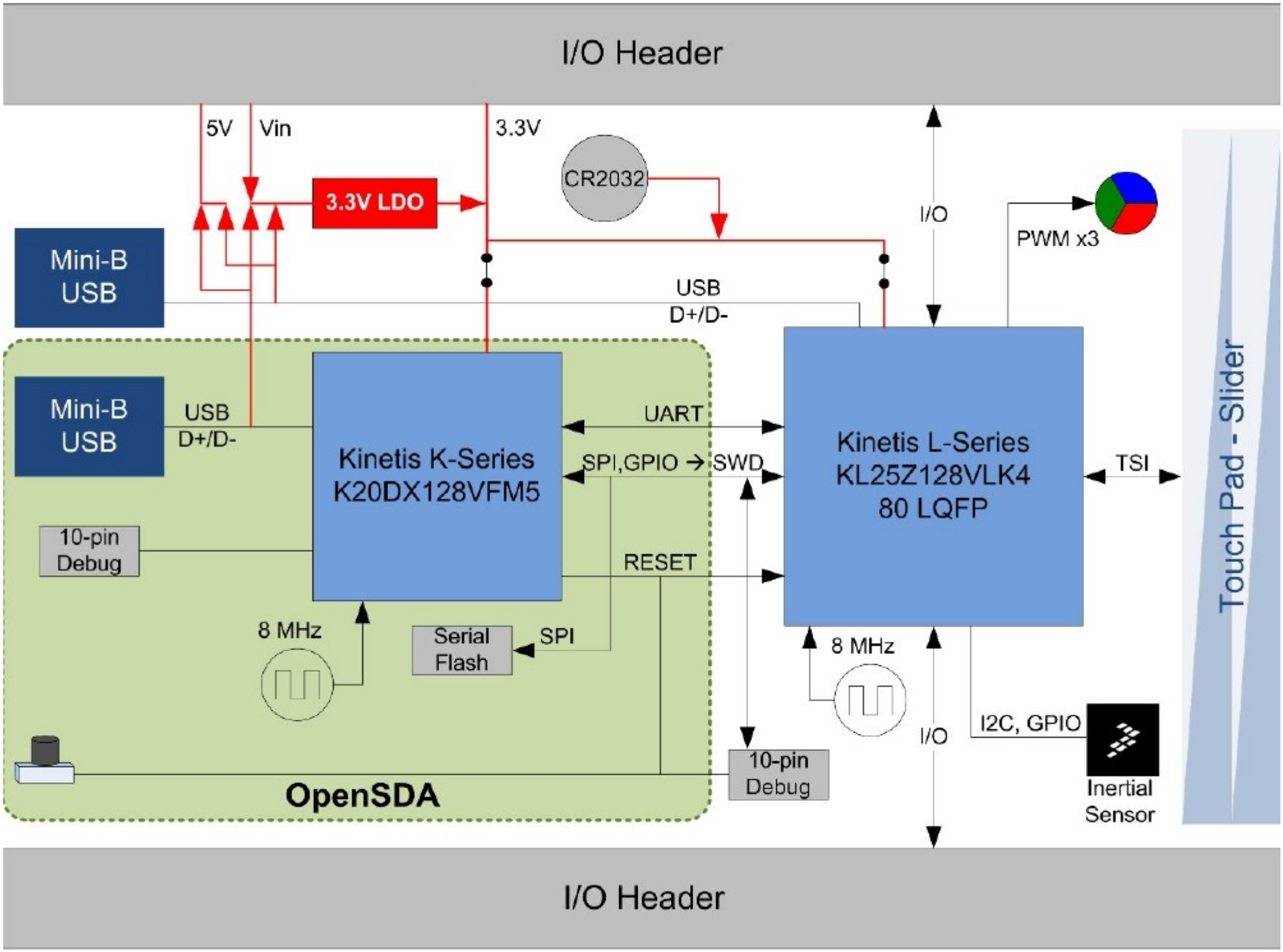
J21
J22
SW1
RST
USB
SDA
SWD
GND
TP1
Y1
Y2
D3
D4
D6
D12
D13


I/O Header
5V
Vin
3.3V
3.3V LDO
CR2032
I/O
PWM x3
Mini-B USB
USB D+/D-
Mini-B USB
USB D+/D-
Kinetis K-Series K20DX128VFM5
UART
SPI,GPIO → SWD
Kinetis L-Series KL25Z128VLK4 80 LQFP
TSI
Touch Pad - Slider
10-pin Debug
RESET
8 MHz
Serial Flash
SPI
8 MHz
I/O
I2C, GPIO
10-pin Debug
Inertial Sensor
OpenSDA
I/O Header