ENGR-355
HW # 1

Due Monday at start of class.

Show your work, neatly, to receive credit. Use data sheets from the class web page.
Tables 5 & 7 of reference [1] on the list of NXP processor documents will be useful.

1) Assume that a SN74LS00 NAND gate is driving several other SN74LS00 gates (one input per gate).
   a) How many gates can it drive?
   b) Calculate the logic high and logic low noise margins

2) Suppose you are given a schematic on which a SN74LS04 invertor is driving a SN74HC00 gate (both powered with 5 volts) and asked if this is a good design. What will your answer be? Could this design be improved and if so how?

3) A KL25Z family micro controller is proposed to create signals for a legacy system built with 74LSxx series logic. The microcontroller runs on 3.3 volts and the legacy system on 5 volts.
   a) Will there be a reasonable noise margin? For analysis assume a standard KL25Z output pin is driving a SN74LS00 NAND gate. Show your work.
   b) Assuming there is a positive noise margin, how many SN74LS00 NAND gate inputs can be driven by a standard GPIO output of the KL25Z family micro controller? (even if the noise margin has ended up negative, answer this loading question)

4) What are the high and low logic level input currents of an SN74HC00 with Vcc=6v? What affects these values?

5) Assume a SN74HC04 gate is driving a number of SN74HC00 gate inputs.
   a) How many gates is it reasonable to drive?
   b) For your answer in part (a), what will be the noise margin?

Use the data sheets on the class web page for the SN74LS00, SN74LS04, and SN74HC00 parts as well as the KL25Z microcontroller.

Submit homework on paper. Show your work.