Effects of Neutrons on Programmable Logic

White Paper

December 2002

Table of Contents

Abstract

Recent industry interest in neutron-induced soft errors has focused primarily on data corruption in memory devices. However, neutron-susceptible memory elements are used for configuration storage in SRAM-based FPGAs. There is a significant and growing risk of functional failure in SRAM-based FPGAs due to the corruption of configuration data. Detection and correction of these configuration upsets is not necessarily instantaneous. In fact, several thousands or millions of clock cycles may pass before the functional failure is detected. For this reason, neutron errors that affect FPGA configuration memory are referred to as “firm errors.” Additionally, schemes to detect and correct FPGA firm errors add extra complexity to the system design and significantly increase board space and bill-of-materials cost. The progression in manufacturing processes to ever deeper sub-micron technologies is increasing the risk of system reliability issues due to neutron effects to the extent that manufacturers of telecommunications and networking systems are developing qualification tests designed to identify components that are susceptible to soft errors. Neutron-induced firm errors contribute significantly to the overall system FIT rate for ground-based and airborne equipment.

Introduction

In the late 1970s and early 1980s, several semiconductor and system companies were experiencing higher than predicted system failure rates due to data corruption in DRAM components. After painstaking research, it was discovered that data corruption resulted from single-event upsets (SEUs) caused by the impact of high-energy neutrons with the SRAM and DRAM components. This paper investigates how these neutrons come into existence, and how they affect semiconductor components and the systems that are built from these components. Additionally, this document offers a detailed analysis on the effect of neutrons on memory cells used to configure FPGAs.

Neutrons – How and Why

High-energy particles from deep space and our sun (galactic cosmic rays and solar rays) collide with atoms of nitrogen and oxygen in the earth's upper atmosphere. The collisions result in the destruction of the nitrogen and oxygen atoms and the production of a variety of other high-energy particles. Most of these particles are charged and recombine quickly. However, a significant portion of the product of atmospheric collisions are neutrons. These neutrons are emitted from the collisions at very high rates and tend not to recombine with other particles, since they are not charged. They travel at high speed until they collide with atmospheric gases, objects on the earth's surface, or objects traveling through the atmosphere.

The number of neutrons, called the "neutron flux," present in the atmosphere depends on several factors, with altitude being the most significant. Neutrons are attenuated by the atmospheric gases, thus decreasing the neutron flux at low altitudes. The peak neutron flux occurs at approximately 60,000 feet. Latitude is also a significant factor in neutron flux. The earth's magnetic field traps cosmic particles and prevents them from colliding with atmospheric gases. The field lines are closer together at the poles, and more cosmic particles are able to penetrate closer to the earth’s surface than at the equator. Hence, there is a significant increase in neutron flux at polar latitudes compared to equatorial latitudes. Additionally, longitude also affects the neutron flux; however, this effect is minor compared to altitude and latitude.

Figure 1 on page 6 illustrates the relationship between altitude and neutron flux. Figure 2 on page 6 illustrates the neutron flux at a variety of altitudes and latitudes. It is interesting to note that the flux density is more than three times higher in Denver than it is in New York. Both cities are on approximately the same latitude, but Denver is located at a much higher altitude.

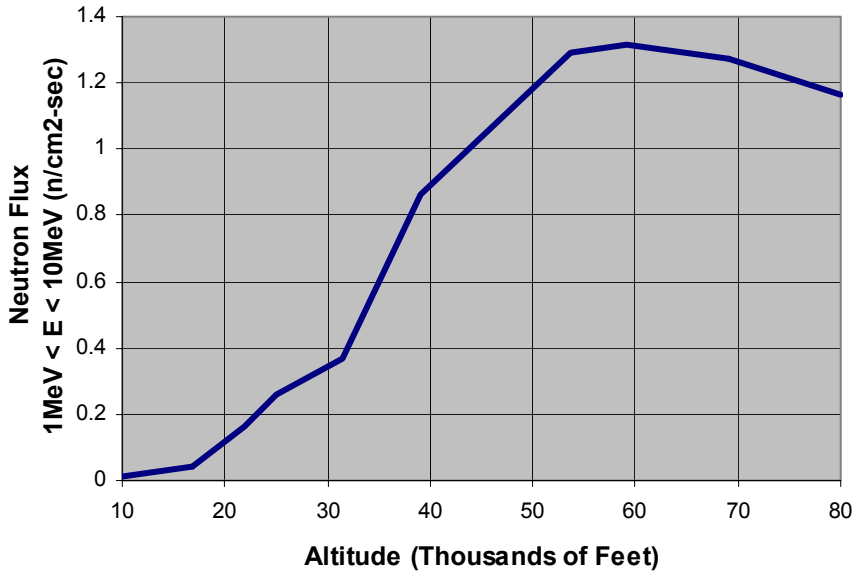

Figure 1: Neutron Flux as a Function of Altitude[1]

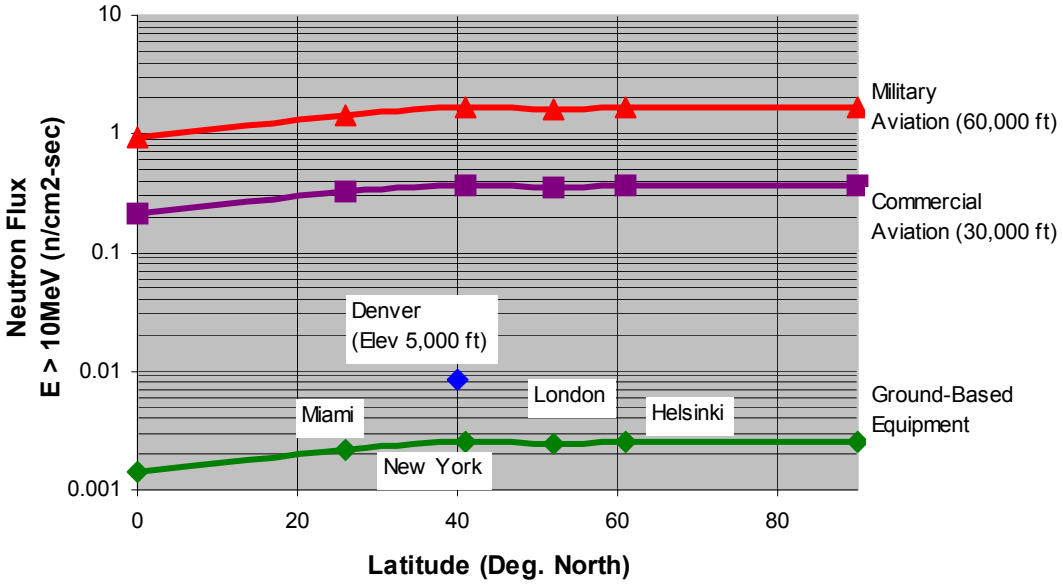

Figure 2: Neutron Flux as a Function of Altitude and Latitude[2]

1. Tabor, A. and E. Normand,1993."Single Event Upsets in Avionics," IEEE Trans Nuclear Science, NS40 (2): 20.
2. "Measurement and Reporting of Alpha Particles and Terrestrial Cosmic Ray Induced Soft Errors in Semiconductor Devices," 2001. JEDEC Standard JESD89.

What Happens When Neutrons Strike Silicon Integrated Circuits?

Neutrons generated by collisions of cosmic particles with nitrogen and oxygen atoms in the upper atmosphere travel at extremely high speeds. Most neutrons striking an integrated circuit will pass through without interacting with the circuit, but occasionally a neutron will pass close enough to a silicon or dopant atom to disturb the atom. The result of this interaction is the creation of secondary particles, which in turn create a trail of electron-hole pairs up to several tens of microns in length. Figure 3 illustrates this interaction. If this occurs near the junction of a reverse-biased pn device in a memory cell or flip-flop, then a voltage spike can occur, resulting in the memory cell or flip-flop changing state. This change of state is frequently referred to as a single-event upset, because it is caused by a single neutron interacting with the crystal lattice of the IC. When the contents of the memory device are changed without damaging the device, it can also be called a "soft error." In such a case, the device can successfully be rewritten with correct data.

It has been observed that the change in state of a memory cell storing device configuration information could create some internal contention within the device or in other devices connected to it, resulting in excessive current and potentially causing damage to the device or in the system. In this way, the threat associated with neutron bombardment is not limited to just soft errors.Corruption of the configuration cell leads to a firm error. In some cases, these firm errors can eventually damage the programming devices, causing a hard error.

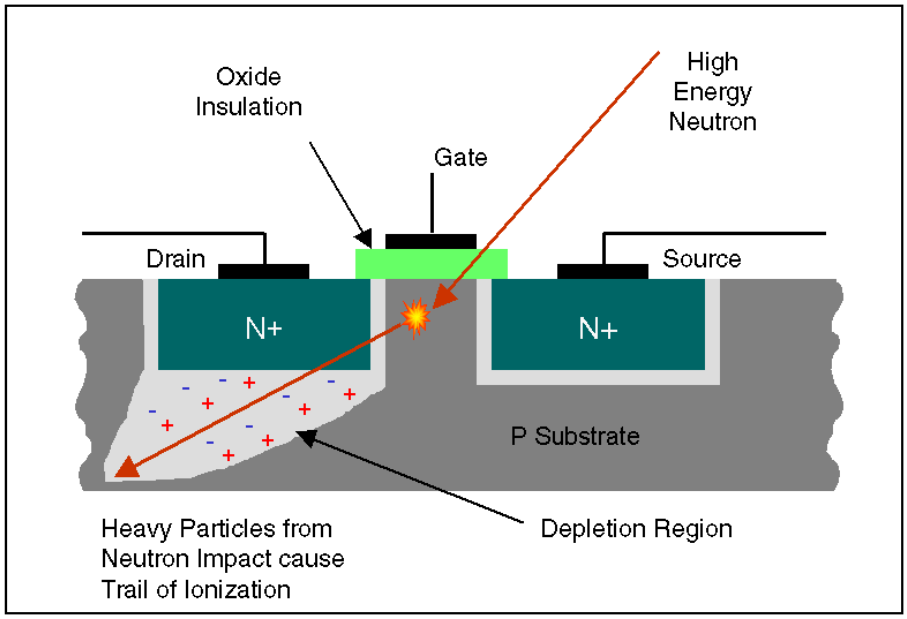

Figure 3: Interaction of a High-Energy Neutron and a Silicon Integrated Circuit

The probability of any given neutron causing a memory cell or a flip-flop to change state is dependent on several factors. The neutron has to enter the silicon with sufficient energy to cause the formation of secondary heavy particles. The ability of a neutron to cause such a reaction depends on its energy level. Secondly, the heavy particles produced by the interaction of the neutron with the silicon lattice must have sufficient energy and must also travel in the right direction to deposit sufficient charge into the sensitive volume of the integrated circuit. Additionally, the sensitivity of an integrated circuit to an upset depends on the process technology. As semiconductor processes advance to smaller feature sizes, the amount of charge required to cause an upset decreases. The number of neutrons capable of causing a reaction that generates the charge required to create an upset increases exponentially as the charge decreases. The relationship between the process technology and the upset rate is illustrated in Figure 4. Note that this chart includes alpha particle effects as well as neutron effects. Alpha particle effects arise from trace amounts of isotopes in the packaging materials. Since the advent of sub-micron technologies, neutron and alpha particle effects have become a much more significant problem. In one sense, the perpetual shrinking of device sizes as IC manufacturers advance from one process to another actually has a mitigating effect. Since the die area occupied by any given memory cell or flip-flop will decrease as the manufacturing process feature size decreases, the probability of a given memory element being struck by a neutron also decreases. However, this is offset by the fact that devices tend to have more memory elements as they migrate to finer process geometries. In addition, the lower energy needed to cause upsets in finer process geometries outweighs the lower probability of an individual element being struck.[3] The net effect is that the probability of a neutron-induced upset increases dramatically as integrated circuits migrate to finer process geometries and smaller feature sizes.

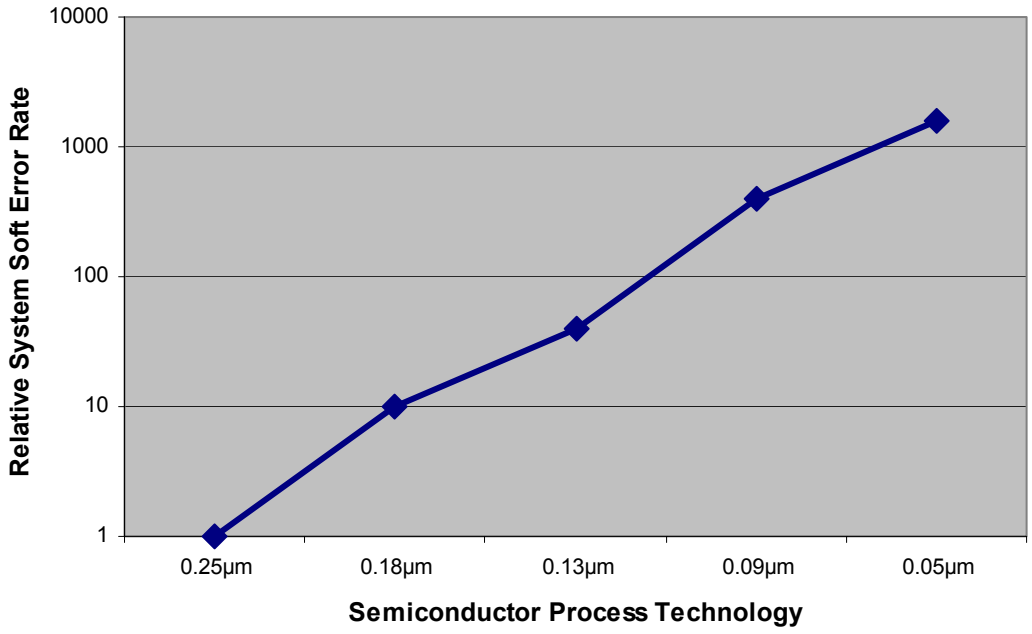

Figure 4: Soft Error Rates as a Function of IC Process Technology[4]

3. Semico Research Corporation, 2002. "Gate Arrays Wane while Standard Cells Soar: ASIC Market Evolution Continues," SC103-02 (June 2002).
4. Semico Research Corporation, "Gate Arrays Wane while Standard Cells Soar: ASIC Market Evolution Continues."

Consequences of Neutron-Induced Single-Event Upsets

The SEUs caused by neutrons inside integrated circuits can occur in memory cells or flip-flops. Most attention has been focused on how to mitigate against data corruption as a result of these SEUs, with techniques such as error detection and correction codes (EDAC) and triple-module redundancy (TMR) being used to detect and overcome SEU-induced soft errors. However, designers using SRAM-based FPGAs face a more serious threat.

SRAM-based FPGAs use 6-transistor SRAM cells to store device configuration information. These cells are only slightly less susceptible to SEUs and soft errors than memory cells typically used for data storage. The consequences of a soft error in one of these configuration cells could be severe. If a neutron causes a configuration bit to upset and change state, it could change the entire functionality of the device. Such a change could result in massive data corruption, the forwarding of spurious signals into other circuits in the system, and in extreme cases, the loss or destruction of a system.

Detection techniques, which rely on reading back the configuration of the FPGA at regular intervals, may let corrupt data enter the system for a significant period of time. In addition, the read-back circuits that enable detection of a corrupted configuration are themselves subject to single-event upsets or damage.[5] Because neutron-induced errors in FPGA configuration memory can have far-reaching consequences beyond transient data corruption, they are referred to as firm errors.

Board-level TMR is sometimes used to mitigate configuration corruption. This uses three instances of the same design programmed into three separate FPGAs with a majority-vote circuit to ensure that data corrupted by single-event upsets are detected before they can be passed through to the rest of the system. The majority vote circuit is normally implemented in SEU-resistant technology. Board-level TMR adds significantly to the complexity of the design and introduces extra expense in the form of component count, board space, and power consumption. Detection of a configuration upset may not happen immediately, since the detect and correct circuits need to cycle through the configuration memory of the SRAM FPGAs. During the time between occurrence and detection of the firm error, the system may be behaving in an unpredictable and uncontrollable manner. Once the firm error has been detected, then it becomes necessary to refresh the configuration of the FPGA. This can take hundreds of milliseconds and may interrupt the operation of the entire system.

As we have seen, the susceptibility of memory devices increases dramatically as the number of memory elements increases and as process technologies shrink. Today's large SRAM-based FPGAs use 0.13µ processing and contain up to 43 million SRAM configuration bits. The only radiation testing on FPGAs of this type for which published data is available was performed on 0.22µ and older devices.[6,7,8,9] It is expected that the susceptibility to neutron-induced upset on the 0.13µ devices is at least four times worse than on the 0.22µ devices of equivalent density. This results from the lower energies required to cause the memory cells to upset.

5. M. Ohlsson, P. Dyreklev, K. Johansson, and P. Alfke, 1998. “Neutron Single Event Upsets in SRAM-based FPGAs,” NSREC.
6. Fuller, E. et al, 1999. “Radiation Test Results of the Virtex FPGA and ZBT SRAM for Space-Based Reconfigurable Computing,” (*MAPLD*, Baltimore MD).
7. Fuller, E. et al, 2000. “Radiation Characterization, and SEU Mitigation, of the Virtex FPGA for Space-Based Reconfigurable Computing,” (*MAPLD*, Baltimore MD).
8. Sturesson, F. and S. Mattsson, 2001. “Radiation Pre-Evaluation of Xilinx FPGA XQVR300,” ESA D-P REP-1091-SE.
9. Sturesson, F. and S. Mattsson, 2001. “Radiation Evaluation of Power-Up Behavior of Xilinx FPGA XQVR300,” ESA D-P REP-1092-SE.

How Often will SRAM-based FPGAs Upset Due to Neutrons?

Data has been published on the susceptibility to upsets of large SRAM-based FPGAs. The most recent data available covers devices with 0.22µ processing. It is expected that devices with finer processing are subject to higher levels of upsets (see the “Consequences of Neutron-Induced Single-Event Upsets” section).

We express failure rates in FITs. A FIT is a "failure in time;" one FIT is a single failure in 1 billion (1E9) hours. Hence, a system that experiences 1 failure in 13,158 hours has a failure rate of 1E9 / 13,158 = 76,000 FITs.

Example 1: Ground-based System with 0.22µ SRAM-based FPGAs

This example analyzes a complex ground-based system. Neutron flux densities were calculated for Denver at an elevation of 5,000 feet using SpaceRad 4.5 (a radiation effects prediction software program). Working from the published radiation data on 0.22µ SRAM-based FPGAs, we have a predicted upset rate of 1.05E-4 upsets per 1M-gate FPGA per day. For a complex ground-based system, such as a telecommunications switch or router, there could be a significant number of 1M-gate FPGAs deployed in the system. For example, a telecommunications switch could have 32 line cards with two 1M-gate FPGAs per card, giving a total of 64 FPGAs per system. Multiplying 1.05E-4 upsets per 1 M-gate device per day by 64 devices, we get 6.73E-3 upsets per system day. This equates to 3,580 hours between system upsets or almost 280,000 FITs.

Example 2: Ground-based System with 0.13µ SRAM-based FPGAs

Using the same system as example 1, we can calculate the upset rate if the system uses 0.13µ FPGAs. A 1M-gate 0.13µ SRAM-based FPGA would be subject to 4.19E-4 upsets per day in this environment. Accordingly, the communications system with 32 line cards and two 1M-gate FPGAs per line card would experience 0.0268 upsets per system day. This equates to 895 hours between system upsets or 1.1 million FITs. A communication network using eight of these switches would experience a system upset every 112 hours, equating to almost 9 million FITs.

Note on examples 1 and 2: a number of telecommunications equipment suppliers have started to require internal qualification procedures to determine susceptibility of integrated circuits to soft errors arising from various radiation sources, including cosmic rays. JEDEC has published a specification covering radiation effects on integrated circuits.[10]

Example 3: Avionics System in Civilian Aviation

This example discusses a circuit board deployed in a system on board a civilian aircraft traveling at an altitude of 30,000 feet on a route about 40 degrees north of the equator (for example, San Francisco to Chicago). The high altitude results in a neutron flux approximately 40 times higher than in the first example. A 1M-gate 0.13µ SRAM-based FPGA would experience 1.85E-2 upsets per day. Supposing that the civilian avionics board uses four of these FPGAs, the board would be subject to 0.074 upsets per day, which equates to 324 hours between upsets or 3 million FITs. Assume there is one of these on board each commercial airliner in service in the USA, and on an average day there may be as many as 4,000 civilian flights in progress at any point in time in the continental USA. The average flight time for a domestic flight in the USA is about three hours. By dividing the total of 12,000 flight-hours by our calculation of 324 hours between upsets, we can estimate that of the 4,000 flights in progress at any point in time, nearly 37 aircraft will experience a neutron-induced SRAM-based FPGA configuration failure during the duration of their flights.

10. “Measurement and Reporting of Alpha Particles and Terrestrial Cosmic Ray Induced Soft Errors in Semiconductor Devices.”

Example 4: Avionics System in Military Aviation

Our example is a circuit board in an avionics system on board a military aircraft flying 40 degrees north of the equator at an altitude of 60,000 feet. The neutron flux in this environment is more than four times higher than the flux in the civilian aircraft flying 30,000 feet lower. This results in an upset rate of 8.33E-2 upsets per day for a 1M-gate 0.13µ SRAM-based FPGA. Again, supposing the avionics board uses four of these FPGAs, the board will experience 0.333 upsets per day, equating to 72 hours between upsets. If the avionics system uses four of these boards, then the time between failures becomes 18 hours.

Table 1 summarizes the Mean Time Between Failures (MTBF) for examples 2, 3, and 4. In addition, the table includes projections for MTBF with 90nm processing. It is expected that neutron-induced soft errors get worse by a factor of two between the 0.13µ and 0.09µ processing nodes. Note that the table ignores Alpha particle effects, which are also expected to be significant at nanometer processing technology nodes and will further decrease the system MTBF.

Table 1 • Projected Mean Time Between Failures Due to Neutron Effects

Scenarios	MTBF (Hours)	
	0.13µ Projection	0.09µ Projection
Ground-based Communication Network	112	58
Civilian Avionics System	324	162
Military Avionics System	18	9

Note on examples 3 and 4: Because of these reliability concerns, avionics systems have historically employed techniques such as system-level redundancy, where flight-critical systems have a backup, which can be employed in case of an emergency. This is practical in avionics systems but is impractical in the case of ground-based equipment, such as medical equipment, industrial control systems, network routers and telecommunication switches. Because of the long qualification cycles associated with high-reliability equipment, avionics systems currently entering service will typically use 0.22µ or older technology. Today, engineers developing systems should be careful to consider the reliability implications of designing 0.18µ or 0.13µ SRAM-based FPGAs into their systems.

Alternatives to SRAM-based FPGAs

Designers who are concerned about the potential system reliability problems associated with FPGA configuration loss due to neutron-induced firm errors should consider Actel FPGAs as an alternative to SRAM FPGAs.

Actel offers a variety of FPGAs which use either Flash or antifuse programmable cells. Both of these programmable technologies were found to withstand bombardment by neutrons at the energy levels typically found in the earth's atmosphere without experiencing configuration loss.[11] They are eminently suitable for applications where reliability is a major concern.

11. For more information concerning the radiation performance of Actel FPGAs, see the following documents:
    - Cronquist, Brian et al, 2000. Radiation-Hardened/High Reliability Programmable Logic Using Modified Commercial off the Shelf: RTSX32S," (*MAPLD*, Baltimore MD).
    - McCollum, John, 1999. "Programmable Elements and Their Impact on FPGA Architecture, Performance, and Radiation Hardness," (*MAPLD*, Baltimore MD).
    - Wang, J. J. et al, 1999. "Total Dose and SEE of Metal-To-Metal Antifuse FPGA," (*MAPLD*, Baltimore MD).
    - Speers, Ted et al, 1999. "0.25µ Flash Memory Based FPGA for Space Applications," (*MAPLD*, Baltimore MD).
    - Wang, J. J. et al, 2000. "Radiation Effects on Flash Memory Based FPGA," (*MAPLD*, Baltimore MD).
    - Wang, J. J. et al, 2001. "Single Event and Total Dose Effects on SEU Hardened Antifuse FPGA," (*MAPLD*, Baltimore MD).
    - Wang, J. J. et al, 2002. "Single Event Effects of a Flash Based FPGA," (*SEE Symposium*, Manhattan Beach CA).
    - Wang, J. J. et al, 2000. "Radiation Tests and Results of a Rad-Tolerant Antifuse FPGA RT54SX," (*RADECS*, Belgium).

Conclusion

Neutrons arising from atmospheric collisions of galactic and solar particles can pose a significant reliability risk for many different types of electronic equipment, both airborne and ground-based. The risk of data corruption in SRAM or DRAM cells can be mitigated with techniques such as EDAC or TMR. However, in many systems today, SRAM-based FPGAs are used for control and data processing functions. These FPGAs use SRAM cells to store the configuration information that gives the devices their functionality. An upset to one of these SRAM cells could potentially result in the FPGA losing its configuration. This is called a firm error. When this occurs, it may cause the host system to malfunction. In ground-based applications where reliability is a concern – medical equipment, radar systems, telecommunications switches and routers – neutron induced functional interrupts could significantly reduce system availability. In airborne applications, where control of aircraft engines, flight control surfaces, and even weapons systems are entrusted to FPGAs, the corruption of the systems' functionality that may result from a configuration firm error could have disastrous consequences.

Neutron-induced firm errors have progressed from being a nuisance to being a significant problem. Future deep submicron manufacturing processes will create substantial challenges for designers of both airborne equipment and ground-based systems. For designers using SRAM-based FPGAs, it will become necessary to implement circuits to detect and correct configuration errors. This will add to system cost and complexity.

Radiation testing data has shown that Actel's antifuse-based and Flash-based FPGAs are not subject to loss of configuration due to neutron-induced upsets. This makes them eminently suitable for applications – both ground-based and airborne – where reliability is a concern.

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Sturesson, F. and S. Mattsson. 2001. Radiation Pre-Evaluation of Xilinx FPGA XQVR30. ESA D-P REP-1091-SE.

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For further reading on this topic, see the following documents:

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