## Pulse Width Modulation Setup

Create a PWM output on PTD5 using TPM0 channel 5. PWM period is to be 20 milliseconds (50 Hz) with pulse length of 1.5 milliseconds.

<u> </u>		page number in reference [2] unless noted as ref [1]	
1)	Turn on bus clocks  Registers: set bits in SIM->SCGC5 and SIM->SCGC6  SIM_SCGC5_PORTD_MASK  SIM_SCGC6_TPM0_MASK		206 208
2)	Configure pin PTD5 for connection to TPM0_ch5 by changing Register: PORTD->PCR[5] which is PCR register bit 5 clear current mux setting by ANDing ~PORT_PCR_M insert desired function using PORT_PCR_MUX(x) who	UX_MASK	184 47[1]
3)	Set clock source for TPM:. TPMSRC and choose PLL (48M) Register: SIM->SOPT2 set 2 bits using SIM_SOPT2_TPMSRC(x) where x set 1 bit using SIM_SOPT2_PLLFLLSEL_MASK	,	196
4)	Make sure timer is turned off (meaning the clock that runs the clock register: TPM0->SC set all bits to zero by writing a zero to this register	counter is off)	552
5)	Set TPM0 channel 5 for edge aligned, high-true pulse, PWM.  Note that 4 bits are involved: MSnB, MSnA, ELSnB, and ELSn more of these bits need to be set they must be set simultaneously and then setting another doesn't work.  Register: TPM0->CONTROLS[5].CnSC where 5 selects set bit MSnB using TPM_CnSC_MSB_MASK set bit ELSnB using TPM_CnSC_ELSB_MASK	y. Setting one	555
6)	Recommendation: Allow the clock to run in debug mode Register: TPM0->CONF set 2 bits using TPM_CONF_DBGMODE(3)		561
7)	Set the prescaler value (select prescale value to obtain Register: TPM0->SC set 3 bits using TPM_SC_PS(value)	n a 3Mhz clock rate)	553
8)	Load MOD register with maximum count to achieve 20msec per TPM0->MOD =	eriod	554
9)	Load CnV register to establish pulse length of 1.5msec TPM0->CONTROLS[5].CnV =		557
10)	Turn on TPM0 (Enable clock)  Register: TPM0->SC and the CMOD field  set 2 bits using TPM_SC_CMOD(x) where it	x can be 0, 1, or 2	553