Engr434 - VLSI Design

Project Documentation

Due Date: 10am, Tuesday, June 9 (Test week)

Final Report Format

• Abstract page
• Introduction (3 pages maximum)
  o System level diagram
  o Design methodology and tradeoffs (ripple carry vs look-ahead carry, etc.)
  o List of utilized resources
    ▪ Mentor Graphics
      o DA-IC
      o IC Station
      o Mosis Analog Design Kit (ADK)
    ▪ Word processor
    ▪ Etc.
• Project overview
  o Signal definitions
  o Block diagrams
  o State machine diagrams, Kmaps, etc.
  o Test results
  o Chip statistics, die size, etc.
• Specifications (6 pages maximum)
  This section should have a short description (including figures) of each functional block of your design i.e. adder, shifter, test circuits, etc.
  o Functional tradeoffs – explain your solution and the tradeoffs in regard to other possible solutions
  o Timing considerations
    ▪ Critical path
    ▪ Frequency maximum/minimum
    ▪ Static vs. dynamic design
    ▪ Etc.
  o Testing - Clearly explain your test strategy
  o Notes on algorithms, if necessary
• Summary (1 page)
• References
• Appendices - the appendices should contain technical data like schematics, layout, timing, and simulation for each cell, and each level of hierarchy.

Your group will prepare a binder (supplied) containing design documentation for your chip. This documentation will be used for chip design, testing, and evaluation. If done properly, it becomes the design reference document. Since team members will be responsible for specific portions of the design, there is individual and group responsibility for sections of the documentation. Documentation should include the following:
Individual Responsibility

Cell Level
- Cell name
- Who is responsible for the schematic
- Who is responsible for the layout
- Functional description - textual, equations, truth table, etc.
- Input signal names
- Output signal names
- Schematic diagram (all levels, if relevant)
- Number of transistors (N and P)
- Simulation results
- Timing and performance summary
  - Delay time (with capacitive load)
  - Rise and fall time (with capacitive load)
- Layout plot
- Cell size

Repeat for all levels of Hierarchy

Group Responsibility

System level
- Functional description and specifications for the design as a whole
- High level block diagram
- Timing diagram and timing specs for the design as a whole
- Layout plot for the whole chip
- Simulation results for the whole chip
- Test vectors used