Introduction to CMOS VLSI Design

Silicon-on-Insulator (SOI)

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Outline

- Overview of Silicon-on-Insulator (SOI)
- Floating Body Voltage
- SOI Advantages
- SOI Disadvantages
- Implications for Circuit Styles
- Summary
SOI Overview

- SOI-based devices differ from conventional silicon-built devices in that the silicon junction is above an electrical insulator, typically silicon dioxide or sapphire (these types of devices are called silicon on sapphire, or SOS). The choice of insulator depends largely on intended application, with sapphire being used for high-performance radio frequency (RF) and radiation-sensitive applications, and silicon dioxide for diminished short channel effects in microelectronics devices.
The implementation of SOI technology is one of several manufacturing strategies employed to allow the continued miniaturization of microelectronic devices, colloquially referred to as extending Moore's Law. Reported benefits of SOI technology relative to conventional silicon (bulk CMOS) processing include:

- **Lower parasitic capacitance** due to isolation from the bulk silicon, which improves power consumption.
- **Resistance to latchup** due to complete isolation of the n- and p-well structures.
- Higher performance at equivalent VDD. Can work at low VDD's.
- Reduced temperature dependency due to no doping.
- Better yield due to high density, better wafer utilization.
- Reduced antenna issues.
- No body or well taps are needed.
- Lower leakage currents due to isolation thus higher power efficiency.
- Inherently radiation hardened (resistant to soft errors), thus reducing the need for redundancy.
SOI Overview

- Adopted for IBM PowerPC µprocessors in 1998
  - Higher performance and lower power than CMOS
  - Higher manufacturing cost and complicated circuit design

- Differences from bulk CMOS
  - Transistor source, drain, & body (channel) surrounded by insulating SiO₂ rather than substrate (well)
  - Eliminates most diffusion parasitic Capacitance
  - Body no longer tied to GND or V_{DD}
    - Any change in body voltage modulates V_t (which has its own advantages and disadvantages)
IBM began to use SOI in the high-end RS64-IV "Istar" PowerPC-AS microprocessor in 2000. Other examples of microprocessors built on SOI technology include AMD's 130 nm, 90 nm, 65 nm, 45 nm and 32 nm single, dual, quad, six and eight core processors since 2001. Freescale adopted SOI in their PowerPC 7455 CPU in late 2001, currently Freescale is shipping SOI products in 180 nm, 130 nm, 90 nm and 45 nm lines. The 90 nm Power Architecture based processors used in the Xbox 360, PlayStation 3 and Wii use SOI technology as well. Competitive offerings from Intel however continues to use conventional bulk CMOS technology for each process node, instead focusing on other venues such as HKMG and Tri-gate transistors to improve transistor performance. In January 2005, Intel researchers reported on an experimental single-chip silicon rib waveguide Raman laser built using SOI.

As for the traditional foundries, on July 2006 TSMC claimed no customer wanted SOI, but Chartered Semiconductor devoted a whole fab to SOI.
Process starts with a wafer containing a thin layer of SiO2 buried beneath a thin single-crystal silicon layer.
IBM SOI Process

- Scanning electron micrograph of a 6-transistor static RAM cell in 0.22 um IBM SOI process
Two Types of SOI

- **Partially depleted (PD)**
  - Body thicker than channel depletion width
  - Body voltage changes, depending on the amount of charge injected into bulk
  - Causes *history effect*, which changes $V_t$

- **Fully depleted (FD)**
  - Body thinner than channel depletion width
  - Fixed body charge
  - Body voltage does not change
  - Thin body makes this very hard to manufacture
  - Therefore, seldom used
Key to understanding SOI is to follow the body voltage
- Body voltage varies as body charges/discharges
- Charge paths to/from floating body
Body Charge Paths

- Reverse-biased drain-to-body $D_{db}$ and source-to-body $D_{sb}$ junctions
  - Carry small diode leakage currents into body
- High-energy carriers cause impact ionization
  - Create $e^-$ hole pairs
    - Injected into gate or gate oxide
    - Cause hot $e^-$ wearout
    - Corresponding holes accumulate in body
  - Most pronounced at $V_{DS} >$ intended operating point
  - $I_{ii}$ is impaction ionization current into body
Ways for Charge to Exit Body

- As body voltage increases
  - Source-to-body $D_{sb}$ junction slightly forward biases
  - Charge exiting from $D_{sb}$ balances charge entering from $D_{db}$

- Rising gate/drain voltage capacitively couples body upward
  - May strongly forward-bias source-to-body $D_{sb}$ junction and spill charge out of body
  - During long idle periods (micro-seconds), body Voltage reaches equilibrium
  - When switching resumes
    - Charge spills off body
    - Shifts body voltage and $V_t$ significantly
SOI Advantages

- Lower $C_{\text{diffusion}}$ – largely eliminated
- Lower parasitic delay
- Lower dynamic power consumption
- Potential for lower $V_t$
  - Bulk CMOS – $V_t$ varies with channel length
    - Poly etching variations cause $V_t$ variations
    - Must make $V_t$ high enough to limit worst-case subthreshold leakage, so nominal $V_t$ is typically higher that needs to be
  - SOI
    - Smaller threshold variations
    - Nominal $V_t$ can be closer to worst-case
    - Faster transistors, especially at low $V_{DD}$
Subthreshold Swing

- Bulk CMOS – subthreshold slope of \( n \nu_T \ln 10 \)
  - \( \nu_T = kT/q \) (thermal voltage, 26 mV at room temp)
  - \( n \) is process dependent, usually about 1.5

- So subthreshold slope is about 90 mV/decade
  - For each 90 mV decrease in \( V_{gs} \) below \( V_t \), subthreshold leakage current is reduced by 10 X

- SOI (IBM) -- subthreshold slope of 75-85 mV/decade

- Double-gate MOSFETs and FINFETs are SOI variations
  - Offer even lower subthreshold slopes
  - Gate surrounds channel – turns off quicker
FINFET’s
SOI is immune to latchup because the insulating oxide eliminates the parasitic bipolar devices that could trigger latchup.
SOI Disadvantages

- **History effect**
  - Changes in body $V$ modulate $V_t$, vary gate delay

- Body voltage depends on whether device was idle or switching -- delay is a function of switching history

- Overall, elevated body voltage
  - Reduces $V_t$ and makes gates faster but the uncertainty makes circuit design more challenging

- **Model history effect**
  - Assign different propagation and contamination delays to each gate
  - History effect causes about 8% gate delay variation (IBM)
    - Less than process and environmental variations
More Disadvantages

- History effect
  - Causes significant mismatches between otherwise matched transistors
    - Sense amplifier (differential pair problems)
    - Analog OPAMP
    - Gilbert cell analog multiplier (mixer)
  - May be solved by introducing substrate contact to make transistor pair behave identically
Parasitic Bipolar Transistor

- Can be a problem because the body/base floats
Current Pulse Problems

- Hold source & drain high for a long time
  - While gate is low
  - Base floats high through diode leakage
- Then, pull source low and *npn* transistor turns ON
  - $I_B$ flows from body/base to source/emitter
  - Causes $\beta I_B$ to flow from drain/collector to source/emitter
    - $\beta$ depends on channel length & doping but can be greater than 1
  - Can get a current pulse from drain to source even though transistor should be OFF
Current Pulse

- This current pulse is sometimes called *Pass-gate Leakage*

- Often happens to OFF pass transistors where source & drain are initially high and then go low
  - No problem for static circuits because the ON transistors oppose the glitch
  - Causes malfunctions in dynamic latches in logic
    - Need strong keepers to hold node steady
Self-Heating Problem

- SiO$_2$ is great thermal and electrical insulator
  - Heat accumulates in transistors
  - Rather than spreading to substrate as in CMOS
- Individual transistors with large power
  - Heat substantially more than the die
  - Deliver less current, slower
- Can raise $T$ by 10 to 15 °C for clock and I/O devices
  - Less significant for logic
Implications for Circuits

- SOI good for fast CMOS logic
  - Smaller $C_{\text{diffusion}}$ gives lower parasitic delay
  - Lower $V_t$ gives better drive current and lower delay

- SOI attractive for low-power design
  - Smaller $C_{\text{diffusion}}$ reduces dynamic power
  - Easier to scale down $V_{DD}$
  - Consider FINFETs – sharper subthreshold slope

- Static CMOS in PD SOI
  - Similar to bulk CMOS family, but faster
  - History effect causes pattern dependent delay variation
Dynamic Gates

- New problem: pass-gate leakage
  - Causes dynamic latches and gates to lose charge on dynamic node
  - Fixed by staticizing the output
Solve Pass-gate Leakage

- Staticize capacitive storage nodes
  - Cross-coupled inverter pair for latches
- pMOS keeper for dynamic gates
  - Can pre-discharge internal nodes to prevent pass-gate leakage
    - Then have a charge sharing problem on internal nodes
- Staticizing transistors must be \( \frac{1}{4} \) as strong as normal path
  - Slows down gates
Gated Clock Problems

- Gated clocks have increased skew
  - History effect makes clock switch more slowly when activated after being disabled for a long time
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