Lecture 5: 
DC & 
Transient Response
Outline

- Pass Transistors
- DC Response
- Logic Levels and Noise Margins
- Transient Response
- RC Delay Models
- Delay Estimation
Activity

1) If the width of a transistor increases, the current will
   increase  decrease  not change

2) If the length of a transistor increases, the current will
   increase  decrease  not change

3) If the supply voltage of a chip increases, the maximum
   transistor current will
   increase  decrease  not change

4) If the width of a transistor increases, its gate capacitance will
   increase  decrease  not change

5) If the length of a transistor increases, its gate capacitance will
   increase  decrease  not change

6) If the supply voltage of a chip increases, the gate capacitance
   of each transistor will
   increase  decrease  not change
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Pass Transistors

- We have assumed source is grounded
- What if source > 0?
  - e.g. pass transistor passing $V_{DD}$
- $V_g = V_{DD}$
  - If $V_s > V_{DD}-V_t$, $V_{gs} < V_t$
  - Hence transistor would turn itself off
- nMOS pass transistors pull no higher than $V_{DD}-V_{tn}$
  - Called a degraded “1”
  - Approaches degraded value slowly (low $I_{ds}$)
- pMOS pass transistors pull no lower than $V_{tp}$
- Transmission gates are needed to pass both 0 and 1
Pass Transistor Ckts

\[ V_{DD} \]

\[ V_{SS} \]

\[ V_{DD} \]

\[ V_{DD} \]

\[ V_{DD} \]

\[ V_{DD} \]

\[ V_{DD} \]
DC Response

- DC Response: $V_{out}$ vs. $V_{in}$ for a gate
- Example: Inverter
  - When $V_{in} = 0 \rightarrow V_{out} = V_{DD}$
  - When $V_{in} = V_{DD} \rightarrow V_{out} = 0$
  - In between, $V_{out}$ depends on transistor size and current
  - By KCL, must settle such that $I_{dsn} = |I_{dsp}|$
  - We could solve equations
  - But graphical solution gives more insight
Transistor Operation

- Current depends on region of transistor behavior
- For what $V_{in}$ and $V_{out}$ are nMOS and pMOS in
  - Cutoff?
  - Linear?
  - Saturation?
## nMOS Operation

<table>
<thead>
<tr>
<th>Cutoff</th>
<th>Linear</th>
<th>Saturated</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{gsn} &lt;$</td>
<td>$V_{gsn} &gt;$</td>
<td>$V_{gsn} &gt;$</td>
</tr>
<tr>
<td>$V_{dsn} &lt;$</td>
<td></td>
<td>$V_{dsn} &gt;$</td>
</tr>
</tbody>
</table>

![nMOS Circuit Diagram](image-url)
### pMOS Operation

<table>
<thead>
<tr>
<th>Cutoff</th>
<th>Linear</th>
<th>Saturated</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{gsp} &gt; V_{tp} )</td>
<td>( V_{gsp} &lt; V_{tp} )</td>
<td>( V_{gsp} &lt; V_{tp} )</td>
</tr>
<tr>
<td>( V_{in} &gt; V_{DD} + V_{tp} )</td>
<td>( V_{in} &lt; V_{DD} + V_{tp} )</td>
<td>( V_{in} &lt; V_{DD} + V_{tp} )</td>
</tr>
<tr>
<td>( V_{dsp} &gt; V_{gsp} - V_{tp} )</td>
<td>( V_{dsp} &lt; V_{gsp} - V_{tp} )</td>
<td>( V_{dsp} &lt; V_{gsp} - V_{tp} )</td>
</tr>
<tr>
<td>( V_{out} &gt; V_{in} - V_{tp} )</td>
<td>( V_{out} &lt; V_{in} - V_{tp} )</td>
<td>( V_{out} &lt; V_{in} - V_{tp} )</td>
</tr>
</tbody>
</table>

\[
V_{gsp} = V_{in} - V_{DD} \quad V_{tp} < 0
\]
\[
V_{dsp} = V_{out} - V_{DD}
\]
Make pMOS wider than nMOS such that $\beta_n = \beta_p$
Current vs. $V_{\text{out}}, V_{\text{in}}$

![Diagram showing current vs. output and input voltage](image)

$V_{\text{in}0}, V_{\text{in}1}, V_{\text{in}2}, V_{\text{in}3}, V_{\text{in}4}, V_{\text{in}5}$

$I_{\text{dsn}}, |I_{\text{dps}}|$
For a given $V_{\text{in}}$:

- Plot $I_{\text{dsn}}$, $I_{\text{dsp}}$ vs. $V_{\text{out}}$
- $V_{\text{out}}$ must be where $|\text{currents}|$ are equal
Load Line Analysis

Load Line Analysis

5: DC and Transient Response  CMOS VLSI Design 4th Ed.
DC Transfer Curve

- Transcribe points onto $V_{in}$ vs. $V_{out}$ plot

![Graph showing DC Transfer Curve with transcribed points and labeling of $V_{in0}$ to $V_{in5}$ and $V_{out}$]
Operating Regions

- Revisit transistor operating regions

<table>
<thead>
<tr>
<th>Region</th>
<th>nMOS</th>
<th>pMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D</td>
<td></td>
<td></td>
</tr>
<tr>
<td>E</td>
<td></td>
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</tbody>
</table>

Diagram:
- Key: A, B, C, D, E
- Labels: $V_{DD}$, $V_{in}$, $V_{out}$, $V_{DD}/2$, $V_{DD} + V_{tp}$
Beta Ratio

- If $\beta_p / \beta_n \neq 1$, switching point will move from $V_{DD}/2$
- Called *skewed* gate

![Diagram showing the effect of beta ratio on the switching point of a gate](image-url)
How much noise can a gate input see before it does not recognize the input?

- **Noise Margins**
  - **Input Characteristics**
    - Logical High Input Range
    - Logical Low Input Range
  - **Output Characteristics**
    - Logical High Output Range
    - Logical Low Output Range

- **Indeterminate Region**
  - \( V_{IH} \)
  - \( V_{IL} \)
  - \( V_{OL} \)
  - \( V_{OH} \)
  - \( V_{DD} \)
  - \( GND \)
Logic Levels

- To maximize noise margins, select logic levels at
  - unity gain point of DC transfer characteristic

\[ V_{DD} \]  
\[ V_{in} \]  
\[ V_{out} \]  
\[ \beta_p/\beta_n > 1 \]
Transient Response

- **DC analysis** tells us $V_{out}$ if $V_{in}$ is constant
- **Transient analysis** tells us $V_{out}(t)$ if $V_{in}(t)$ changes
  - Requires solving differential equations
- Input is usually considered to be a step or ramp
  - From 0 to $V_{DD}$ or vice versa
Inverter Step Response

- Ex: find step response of inverter driving load cap

\[ V_{in}(t) = \]

\[ V_{out}(t < t_0) = \]

\[ \frac{dV_{out}(t)}{dt} = \]

\[ I_{dsn}(t) = \begin{cases} 
\frac{V_{in}(t)}{C_{load}} & t \leq t_0 \\
\frac{V_{out}}{C_{load}} & V_{out} > V_{DD} - V_t \\
\frac{V_{out}}{C_{load}} & V_{out} < V_{DD} - V_t 
\end{cases} \]
Delay Definitions

- $t_{pdr}$: rising propagation delay
  - From input to rising output crossing $V_{DD}/2$

- $t_{pdf}$: falling propagation delay
  - From input to falling output crossing $V_{DD}/2$

- $t_{pd}$: average propagation delay
  - $t_{pd} = (t_{pdr} + t_{pdf})/2$

- $t_r$: rise time
  - From output crossing 0.2 $V_{DD}$ to 0.8 $V_{DD}$

- $t_f$: fall time
  - From output crossing 0.8 $V_{DD}$ to 0.2 $V_{DD}$
Delay Definitions

- $t_{c_{dr}}$: rising contamination delay
  - From input to rising output crossing $V_{DD}/2$
- $t_{c_{df}}$: falling contamination delay
  - From input to falling output crossing $V_{DD}/2$
- $t_{c_{d}}$: average contamination delay
  - $t_{pd} = (t_{c_{dr}} + t_{c_{df}})/2$
Simulated Inverter Delay

- Solving differential equations by hand is too hard
- SPICE simulator solves the equations numerically
  - Uses more accurate I-V models too!
- But simulations take time to write, may hide insight

![Diagram of inverter delay with labels](image_url)

- $V_{in}$
- $V_{out}$
- $t_{pd}$ = 66ps
- $t_{pdr}$ = 83ps

5: DC and Transient Response  CMOS VLSI Design 4th Ed.
Delay Estimation

- We would like to be able to easily estimate delay
  - Not as accurate as simulation
  - But easier to ask “What if?”
- The step response usually looks like a 1st order RC response with a decaying exponential.
- Use RC delay models to estimate delay
  - C = total capacitance on output node
  - Use effective resistance \( R \)
  - So that \( t_{pd} = RC \)
- Characterize transistors by finding their effective \( R \)
  - Depends on average current as gate switches
Effective Resistance

- Shockley models have limited value
  - Not accurate enough for modern transistors
  - Too complicated for much hand analysis
- Simplification: treat transistor as resistor
  - Replace $I_{ds}(V_{ds}, V_{gs})$ with effective resistance $R$
    - $I_{ds} = V_{ds}/R$
  - $R$ averaged across switching of digital gate
- Too inaccurate to predict current at any given time
  - But good enough to predict RC delay
RC Delay Model

- Use equivalent circuits for MOS transistors
  - Ideal switch + capacitance and ON resistance
  - Unit nMOS has resistance $R$, capacitance $C$
  - Unit pMOS has resistance $2R$, capacitance $C$
- Capacitance proportional to width
- Resistance inversely proportional to width
RC Values

- Capacitance
  - $C = C_g = C_s = C_d = 2 \text{ fF/}\mu\text{m}$ of gate width in 0.6 \(\mu\text{m}\)
  - Gradually decline to 1 fF/\(\mu\text{m}\) in 65 nm

- Resistance
  - $R \approx 10 \text{ K}\Omega \cdot \mu\text{m}$ in 0.6 \(\mu\text{m}\) process
  - Improves with shorter channel lengths
  - 1.25 K\Omega \cdot \mu\text{m}$ in 65 nm process

- Unit transistors
  - May refer to minimum contacted device (4/2 \(\lambda\))
  - Or maybe 1 \(\mu\text{m}\) wide device
  - Doesn’t matter as long as you are consistent
Inverter Delay Estimate

- Estimate the delay of a fanout-of-1 inverter

\[ d = 6RC \]
Delay Model Comparison

![Graph showing delay model comparison](image-url)
Example: 3-input NAND

Sketch a 3-input NAND with transistor widths chosen to achieve effective rise and fall resistances equal to a unit inverter (R).
Annotate the 3-input NAND gate with gate and diffusion capacitance.
Elmore Delay

- ON transistors look like resistors
- Pullup or pulldown network modeled as RC ladder
- Elmore delay of RC ladder

\[ t_{pd} \approx \sum_{\text{nodes } i} R_{i \rightarrow \text{source}} C_i \]

\[ = R_1 C_1 + (R_1 + R_2) C_2 + \ldots + (R_1 + R_2 + \ldots + R_N) C_N \]
Example: 3-input NAND

- Estimate worst-case rising and falling delay of 3-input NAND driving \( h \) identical gates.

\[
t_{\text{pdr}} = (9 + 5h)RC
\]

\[
t_{\text{pdf}} = (3C)\left(\frac{R}{3}\right) + (3C)\left(\frac{R}{3} + \frac{R}{3}\right) + \left[(9 + 5h)C\right]\left(\frac{R}{3} + \frac{R}{3} + \frac{R}{3}\right)
\]

\[
= (12 + 5h)RC
\]
Delay Components

- Delay has two parts
  - *Parasitic delay*
    - 9 or 12 RC
    - Independent of load
  - *Effort delay*
    - 5h RC
    - Proportional to load capacitance
Contamination Delay

- Best-case (contamination) delay can be substantially less than propagation delay.
- Ex: If all three inputs fall simultaneously

\[ t_{cdr} = \left[ (9 + 5h)C \right] \left( \frac{R}{3} \right) = \left( 3 + \frac{5}{3}h \right) RC \]
Diffusion Capacitance

- We assumed contacted diffusion on every s/d.
- Good layout minimizes diffusion area
- Ex: NAND3 layout shares one diffusion contact
  - Reduces output capacitance by 2C
  - Merged uncontacted diffusion might help too
Which layout is better?
Summary

- Pass Transistors
- DC Response
- Logic Levels and Noise Margins
- Transient Response
- RC Delay Models
- Delay Estimation