ADK v3.1
ADK v3.0

MOSIS Scalable CMOS Submicron Design Rules (as of Rev. 7.3 with half lambda rules)

UNIT LENGTH u
UNIT CAPACITANCE ff
UNIT RESISTANCE ohm
UNIT TIME ns

INCLUDE "$ADK/technology/ic/process/layers_ami05"

DRC_0 = EXTENT
BULK = SIZE DRC_0 BY 1.0

PSUB = BULK NOT NWELL
DIFF = ACTIVE NOT POLY
PDIFF = DIFF AND P_PLUS_SELECT
NDIFF = DIFF AND N_PLUS_SELECT
NWTIE = NDIFF AND NWELL
PSUBTIE = PDIFF AND PSUB
GATES = POLY AND ACTIVE
NGATE = GATES AND N_PLUS_SELECT
PGATE = GATES AND P_PLUS_SELECT

SGATES = SIZE GATES BY 2
GPOLY = POLY AND SGATES
FPOLY = POLY NOT GPOLY

dfcnt = CONTACT_TO_ACTIVE INSIDE DIFFUSED_RESISTOR
dfcnto = size dfcnt by 2
dfrs = dfr NOT dfcnto
psdt = pdiff not poly
nsdt = ndiff not poly
PSRCDRN = psdt not dfrs
NSRCDRN = nsdt not dfrs

HR = ELECTRODE AND HI_RES_IMPLANT
HR_pin = ELECTRODE NOT HI_RES_IMPLANT

CAP = POLY AND ELECTRODE
CAP_pin = METAL1 AND ELECTRODE

SELECT = N_PLUS_SELECT OR P_PLUS_SELECT
BOTH_CONTACT = CONTACT_TO_POLY OR CONTACT_TO_ACTIVE

CONNECT METAL2 METAL3 BY VIA2
CONNECT METAL1 METAL2 BY VIA
CONNECT METAL1 POLY BY CONTACT_TO_POLY
CONNECT METAL3 METAL3.PORT
CONNECT METAL2 METAL2.PORT
CONNECT METAL1 METAL1.PORT
//CONNECT POLY

CONNECT METAL1 HR_pin by CONTACT_TO_ELECTRODE

CONNECT METAL1 ACTIVE by CONTACT_TO_ACTIVE DIRECT
CONNECT METAL1 N_WELL P_WELL by CONTACT_TO_ACTIVE DIRECT

//
// Mask ICtrace Rules
//
CONNECT METAL1 NSRCDRN PSRCDRN by CONTACT_TO_ACTIVE mask
CONNECT PSRCDRN PSUB mask
CONNECT NSRCDRN NWELL mask
CONNECT N_PLUS_SELECT mask
CONNECT P_PLUS_SELECT mask
CONNECT NPLUS mask
CONNECT PPLUS mask

VIRTUAL CONNECT NAME VSS
VIRTUAL CONNECT NAME Ring_VSS
VIRTUAL CONNECT NAME VDD
VIRTUAL CONNECT NAME Ring_VDD
VIRTUAL CONNECT NAME GND
VIRTUAL CONNECT NAME ground

//
// Technology specific information.
//

//
// ICtrace Device Definitions
//

DEVICE MP PGATE POLY(G) PSRCDRN(S) PSRCDRN(D) NWELL(B) (S D) NETLIST MODEL p [ prop w, l, AS, AD
  w = ( perim_co(pgate,s) + perim_co(pgate,d) ) * 0.15 // factor is .5 * lambda
  l = ( perim(pgate) - perim_co(pgate,s) - perim_in(pgate,s) - perim_co(pgate,d) - perim_in(pgate,d) ) * 0.15
  AS = area(S) * 0.09
  AD = area(D) * 0.09
]

DEVICE MN NGATE POLY(G) NSRCDRN(S) NSRCDRN(D) PSUB(B) (S D) NETLIST MODEL n [ prop w, l, AS, AD
  w = ( perim_co(ngate,s) + perim_co(ngate,d) ) * 0.15 // factor is .5 * lambda
\[
1 = (\text{perim}(\text{ngate}) - \text{perim}_{co}(\text{ngate},s) - \text{perim}_{in}(\text{ngate},s) - \text{perim}_{co}(\text{ngate},d) - \text{perim}_{in}(\text{ngate},d)) \times 0.15
\]
\[
\text{AS} = \text{area}(S) \times 0.09
\]
\[
\text{AD} = \text{area}(D) \times 0.09
\]
DEVICE C CAP POLY CAP_pin (POS NEG) [0.0806 0]

// DEVICE R pres respin respin [25.7]

DEVICE R HR HR_pin HR_pin [1253.5]

//
// ICextract Rule Definitions
//
capacitance order       POLY METAL1 METAL2 METAL3 direct mask

capacitance intrinsic METAL3 [0.0014 0.0135]
capacitance intrinsic METAL2 [0.0020 0.0198]
capacitance intrinsic METAL1 [0.0036 0.0237]
capacitance intrinsic POLY [0.0078 0]

capacitance crossover METAL3 METAL2 [0.0029 0.0156 0]
capacitance crossover METAL3 METAL1 [0.0015 0.0120 0]
capacitance crossover METAL3 POLY [0.0013 0.0108 0]
capacitance crossover METAL2 METAL1 [0.0029 0.0162 0]
capacitance crossover METAL2 POLY [0.0020 0.0141 0]
capacitance crossover METAL1 POLY [0.0048 0.0201 0]

resistance sheet       METAL3 [0.05 0]
resistance sheet       METAL2 [0.09 0]
resistance sheet       METAL1 [0.10 0]
resistance sheet       POLY [25.7 0]
resistance sheet       HR_pin [26.7 0]
resistance sheet       PSRCDRN [101.1 0]
resistance sheet       NSRCDRN [81.8 0]

resistance connection METAL1 POLY [18.5 0]
resistance connection METAL1 HR_pin [18.0 0]
resistance connection METAL1 METAL2 [1.48 0]
resistance connection METAL2 METAL3 [0.94 0]
resistance connection METAL1 PSRCDRN [110.0 0]
resistance connection METAL1 NSRCDRN [53.2 0]

//
// END OF TECHNOLOGY SPECIFIC INFORMATION
//
// ICrules Rule Definitions
//
subcont = EXT CONTACT_TO_ACTIVE (active) < 2 ABUT == 0 OVERLAP OPPOSITE
wellcont = EXT CONTACT_TO_ACTIVE (active) < 2 ABUT == 0 OVERLAP OPPOSITE

bad_active_area { @ Active area must be covered by a select
  x = active NOT P_PLUS_SELECT
  x NOT N_PLUS_SELECT
}

bad_contact_poly { @ Contact to poly must consist of poly, CONTACT_TO_POLY, and METAL1
  CONTACT_TO_POLY NOT INSIDE poly
  CONTACT_TO_POLY NOT INSIDE METAL1
}

bad_contact_ELECTRODE { @ Contact to ELECTRODE must consist of ELECTRODE, CONTACT_TO_ELECTRODE, and METAL1
  CONTACT_TO_ELECTRODE NOT INSIDE ELECTRODE
  CONTACT_TO_ELECTRODE NOT INSIDE METAL1
}

bad_contact_active { @ Contact to active must consist of active, CONTACT_TO_ACTIVE, and METAL1
  CONTACT_TO_ACTIVE NOT INSIDE active
  CONTACT_TO_ACTIVE NOT INSIDE METAL1
}

bad_contact_gate { @ Contact to poly may not be on gate region.
  CONTACT_TO_POLY AND active
}

bad_via { @ Via must consist of METAL1, via, and METAL2
  via NOT INSIDE METAL1
  via NOT INSIDE METAL2
}

bad_via2 { @ Via2 must consist of METAL2, via, and METAL3
  via2 NOT INSIDE METAL2
  via2 NOT INSIDE METAL3
}

select_overlap { @ Overlap of N+ and P+ not allowed
  AND P_PLUS_SELECT N_PLUS_SELECT
}

bad_nwell { @ Nwell must have well contact
  x = CONTACT_TO_ACTIVE AND nwtie
  nwell NOT ENCLOSE x
}

bad_psubstrate { @ Psubstrate must have a substrate contact
  x = CONTACT_TO_ACTIVE AND psubtie
  psub NOT ENCLOSE x
}

bad_pgate { @ P-type gate must not be in psubstrate
  pgate AND psub
}

bad_ngate { @ N-type gate must not be in nwell
  ngate AND nwell
}

bad_port { @ Port must be completely covered with Metal
  METAL1.PORT NOT INSIDE METAL1
  METAL2.PORT NOT INSIDE METAL2
  METAL3.PORT NOT INSIDE METAL3
}
DRC1_1 { @ N-Well width = 12L
  INT nwell < 12 SQUARE REGION SINGULAR
}

DRC1_2 { @ N-well spacing (different potential) = 18L
  EXT nwell < 18 NOT CONNECTED SQUARE REGION SINGULAR
}

DRC2_1 { @ Active area width = 3L
  INT active < 3 SQUARE REGION
}

DRC2_2 { @ Active area spacing = 3L
  EXT active < 3 SQUARE REGION
}

DRC2_3 { @ Source/Drain Active to Well Edge = 6L
  EXT nwell ndiff < 6 SQUARE REGION SINGULAR
  ENC pdiff nwell < 6 ABUT == 0 OVERLAP SQUARE REGION SINGULAR
}

DRC2_4 { @ Substrate/Well Contact, Active to Well Edge = 3L
  ENC ndiff nwell < 3 ABUT == 0 OVERLAP REGION SINGULAR
  EXT nwell pdiff < 3 REGION SINGULAR
}

DRC3_1 { @ Poly width = 2L
  INT poly < 2 SINGULAR
}

DRC3_2 { @ Poly spacing = 3L
  EXT poly < 3 SINGULAR
}

DRC3_3 { @ Gate poly overlap of active = 2L
  pgate TOUCH psrcdrn == 1
  ngate TOUCH nsrscdrn == 1
  ENC active poly < 2 ABUT == 0 SQUARE REGION
}

DRC3_4 { @ Active overlap of gate poly = 3L
  ENC poly active < 3 ABUT == 0 SQUARE REGION
}

DRC3_5 { @ Field poly to active = 1L
  EXT poly active < 1 SQUARE REGION ABUT == 0
}

DRC4.1p {
  nxtor = NSRCDRN OR GATES
  ENCLOSURE GATES nxtor < 3
} // nselect overlap of gate

DRC4.1n {
  pxtor = PSRCDRN OR GATES
  ENCLOSURE GATES pxtor < 3
} // pselect overlap of gate

DRC4.2 {
  ENCLOSURE ACTIVE SELECT < 2 ABUT == 0 OVERLAP SINGULAR
} // select overlap of active
  // use of both selects implies space

DRC4.3p {
  ENCLOSURE CONTACT_TO_ACTIVE P_PLUS_SELECT < 1 ABUT == 0 OVERLAP
  SINGULAR
} // pselect overlap of actcont

DRC4.3n {

ENCLOSURE CONTACT_TO_ACTIVE N_PLUS_SELECT < 1 ABUT == 0 OVERLAP
SINGULAR
} // nselect overlap of acctcont
DRC4.4pw { INTERNAL P_PLUS_SELECT < 2 }  // width
DRC4.4ps {
  EXTERNAL P_PLUS_SELECT < 2 NOT CONNECTED
}   // space
DRC4.4nw { INTERNAL N_PLUS_SELECT < 2 }  // width
DRC4.4ns {
  EXTERNAL N_PLUS_SELECT < 2 NOT CONNECTED
}   // space
DRC4.5np { AND N_PLUS_SELECT P_PLUS_SELECT } // p and n selects overlap

DRC5_1 { @ Contact to poly size exactly 2L X 2L
  NOT RECTANGLE CONTACT_TO_POLY == 2 BY == 2
}
//
// This rule is violated in MOSIS pads. This rule set utilizes the half
// lambda grid rules. Therefore, to ignore the violation, a new layer
// (PADS) has been introduced to ignore this violation if present.
//
DRC5_2 { @ Poly overlap for contact = 1.5L
  x = CONTACT_TO_POLY NOT PADS
  ENC x poly < 1.5 ABUT == 0 OVERLAP REGION OVERLAP
}
DRC5_3 { @ Contact to poly spacing = 3L
  EXT CONTACT_TO_POLY < 3 SINGULAR SQUARE
}
DRC5_4 { @ Contact to active space to gate of transistor = 2L
  EXT CONTACT_TO_POLY gates < 2 ABUT == 0 OVERLAP REGION SINGULAR
}
DRC6_1 { @ Contact to active exactly 2L X 2L
  NOT RECTANGLE CONTACT_TO_ACTIVE == 2 BY == 2
}
//
// This rule is violated in MOSIS pads. This rule set utilizes the half
// lambda grid rules. Therefore, to ignore the violation, a new layer
// (PADS) has been introduced to ignore this violation if present.
//
DRC6_2 { @ Active overlap for contact = 1.5L
  x = CONTACT_TO_ACTIVE NOT PADS
  ENC x active < 1.5 ABUT == 0 OVERLAP REGION
}
DRC6_3 { @ Contact to active spacing = 3L
  EXT CONTACT_TO_ACTIVE < 3 SINGULAR SQUARE REGION
}
DRC6_4 { @ Contact to active space to gate of transistor = 2L
  EXT CONTACT_TO_ACTIVE gates < 2 ABUT == 0 OVERLAP REGION
SINGULAR
}
DRC7_1 { @ Metall width = 3L
  INT METALL < 3 SINGULAR
}
DRC7_2 { @ Metal1 spacing = 3L
    EXT METAL1 < 3 SINGULAR
}
DRC7_3 { @ Metal1 overlap of contact to poly or contact to active = 1L
    ENC BOTH_CONTACT METAL1 < 1 ABUT == 0 SQUARE REGION
}
DRC7_4 { @ Metal1 spacing = 6L if width > 10L
    widem = METAL1 WITH WIDTH > 10
    thinm = METAL1 WITH WIDTH <= 10
    EXT widem < 6 SINGULAR
    EXT widem thinm < 6 SINGULAR
}
DRC8_1 { @ Via size exactly 2L X 2L
    x = NOT RECTANGLE via == 2 BY == 2
    x OUTSIDE overglass
}
DRC8_2 { @ Via spacing = 3L
    EXT via < 3 SINGULAR SQUARE REGION
}
DRC8_3 { @ Via overlap by METAL1 = 1L
    ENC via METAL1 < 1 ABUT == 0 SQUARE REGION
}
DRC9_1 { @ Metal2 width = 3L
    INT METAL2 < 3 SINGULAR
}
DRC9_2 { @ Metal2 spacing = 3L
    EXT METAL2 < 3 SINGULAR
}
DRC9_3 { @ Metal2 overlap of via = 1L
    ENC via METAL2 < 1 ABUT == 0 SQUARE REGION
}
DRC9_4 { @ Metal2 spacing = 6L if width > 10L
    widem = METAL2 WITH WIDTH > 10
    thinm = METAL2 WITH WIDTH <= 10
    EXT widem < 6 SINGULAR
    EXT widem thinm < 6 SINGULAR
}
DRC11_1 { @ ELECTRODE width = 7L ON CAP
    INT CAP < 7 SQUARE REGION SINGULAR
}
DRC11_2 { @ ELECTRODE spacing = 3L
    EXT CAP < 3 SQUARE REGION SINGULAR
}
DRC11_3 { @ Poly overlap of ELECTRODE = 5L
    ENC CAP poly < 5 ABUT == 0 SQUARE REGION OVERLAP
}
DRC11_4 { @ ELECTRODE spacing to active or well = 2L
    EXT CAP active < 2 SQUARE REGION SINGULAR
    EXT CAP nwell < 2 SQUARE REGION SINGULAR
}
DRC11_5 { @ ELECTRODE spacing to Contact to Poly = 6L ON CAP
    EXT CAP CONTACT_TO_POLY < 6 SQUARE REGION SINGULAR
}
DRC11_sel { @ Capacitor and Select may not intersect
x = poly TOUCH cap
y = ELECTRODE TOUCH cap
z = x OR y
  z AND N_PLUS_SELECT
  z AND P_PLUS_SELECT
}

DRC12_1 { @ ELECTRODE width = 2L
  x = ELECTRODE NOT cap
  EXT x < 2 SQUARE REGION SINGULAR
}

DRC12_2 { @ ELECTRODE spacing = 3L
  EXT ELECTRODE < 3 SQUARE REGION SINGULAR
}

DRC13_1 { @ Contact to ELECTRODE size exactly 2L X 2L
  NOT RECTANGLE CONTACT_TO_ELECTRODE == 2 BY == 2
}

DRC13_2 { @ Contact to ELECTRODE spacing = 3L
  EXT CONTACT_TO_ELECTRODE < 3 SQUARE SINGULAR
}

DRC13_3 { @ ELECTRODE overlap for contact = 3L ON CAP PLATE
  x = cap AND CONTACT_TO_ELECTRODE
  ENC x ELECTRODE < 3 ABUT == 0 SQUARE REGION OVERLAP
}

DRC13_4 { @ ELECTRODE overlap for contact = 2L NOT ON CAP PLATE
  x = CONTACT_TO_ELECTRODE NOT cap
  ENC x ELECTRODE < 2 ABUT == 0 SQUARE REGION OVERLAP
}

DRC13_5 { @ Contact to ELECTRODE space to Poly or Active = 3L
  EXT CONTACT_TO_ELECTRODE poly < 3 SQUARE REGION SINGULAR
  EXT CONTACT_TO_ELECTRODE active < 3 SQUARE REGION SINGULAR
}

DRC14_1 { @ Via2 size exactly 2L X 2L
  x = NOT RECTANGLE via2 == 2 BY == 2
  x OUTSIDE overglass
}

DRC14_2 { @ Via2 spacing = 3L
  EXT via2 < 3 SINGULAR SQUARE REGION
}

DRC14_3 { @ Via2 overlap by METAL2 = 1L
  ENC via2 METAL2 < 1 ABUT == 0 SQUARE REGION
}

DRC14_4 { @ Via2 spacing to via = 2L
  EXT via via2 < 2 ABUT == 0 OVERLAP SQUARE REGION SINGULAR
  ENC via via2 < 2 ABUT == 0 SQUARE REGION SINGULAR
}

DRC15_1 { @ Metal3 width = 5L
  INT metal3 < 5 SINGULAR
}

DRC15_2 { @ Metal3 spacing = 3L
  EXT metal3 < 3 SINGULAR
}

DRC15_3 { @ Metal3 overlap of via2 = 2L
  ENC via2 metal3 < 2 ABUT == 0 SQUARE REGION
}
DRC15_4 { @ Metal3 spacing = 6L if width > 10L
    widem = METAL3 WITH WIDTH > 10
    thinm = METAL3 WITH WIDTH <= 10
    EXT widem < 6 SINGULAR
    EXT widem thinm < 6 SINGULAR
}

DRC27_1 { @ HI_RES_IMPLANT width = 4L
    INT hi_res_implant < 4 SINGULAR
}

DRC27_2 { @ HI_RES_IMPLANT spacing = 4L
    EXT hi_res_implant < 4 SINGULAR
}

DRC27_3 { @ HI_RES_IMPLANT spacing to contact = 2L
    EXT hi_res_implant contact_to_electrode < 2 ABUT == 0 OVERLAP
    SQUARE REGION SINGULAR
    ENC hi_res_implant contact_to_electrode < 2 ABUT == 0 SQUARE
    REGION SINGULAR
}

DRC27_4 { @ HI_RES_IMPLANT spacing to active = 2L
    EXT hi_res_implant active < 2 ABUT == 0 OVERLAP SQUARE REGION
    SINGULAR
    ENC hi_res_implant active < 2 ABUT == 0 SQUARE REGION SINGULAR
}

DRC27_9 { @ HI_RES_IMPLANT overlap of electrode = 2L
    ENC HI_RES_IMPLANT electrode < 2 ABUT == 0 SQUARE REGION
}

//
// Miscellaneous
//
TEXT LAYER METAL1.PORT
TEXT LAYER METAL2.PORT
TEXT LAYER METAL3.PORT
ATTACH METAL1.PORT METAL1 mask
ATTACH METAL2.PORT METAL2 mask
ATTACH METAL3.PORT METAL3 mask

PORT LAYER TEXT METAL1.PORT
PORT LAYER TEXT METAL2.PORT
PORT LAYER TEXT METAL3.PORT

LVS Abort on Supply Error  NO
//LVS FILTER sch_filter_direct_open OPEN SOURCE DIRECT
//LVS FILTER sch_filter_direct_short SHORT SOURCE DIRECT
//LVS FILTER sch_filter_mask_open OPEN SOURCE MASK
//LVS FILTER sch_filter_mask_short SHORT SOURCE MASK
//LVS FILTER lay_filter_direct_open OPEN LAYOUT DIRECT
//LVS FILTER lay_filter_direct_short SHORT LAYOUT DIRECT
// Filter out all Voltage and Current sources from LVS reports
LVS FILTER v OPEN
LVS FILTER i OPEN
LVS FILTER e OPEN
LVS FILTER f OPEN
LVS FILTER g OPEN

GROUP CONTINUOUS_DRC
  DRC3_1
  DRC3_2
  DRC7_1
  DRC7_2
  DRC9_1
  DRC9_2
  DRC15_1
  DRC15_2