This test will be open book and 60 minutes in length. Presented below is a topical review of material covered since the start of the quarter, not necessarily in the order presented.

**Current News Topics**
1. State of Technology
2. Companies Making News

**Lab**
1. Schematic Issues
2. Simulation
3. Layout
4. Verification
   a. LVS
   b. DRC
5. Project

**Chapter 1 – Introduction**
1. A Brief History
2. MOS Transistors
3. CMOS Logic
4. CMOS Fabrication

**Chapter 2 – MOS Transistor Theory**
1. Long-Channel I-V Characteristics
2. Three Operational Regions – Cutoff, Linear, Saturation
3. Non-ideal I-V Effects
   a. Mobility Degradation and Velocity Saturation
   b. Channel Length Modulation
   c. Body Effect
   d. Drain-Induced Barrier Lowering
   e. Short Channel Effects
   f. Leakage
      i. Sub-Threshold
      ii. Gate
      iii. Junction
4. DC Response
   a. Beta Ratio Effects
   b. Noise Margin

**Chapter 4 – Delay**
1. Definitions – Propagation, Contamination, Rise and Fall Times
2. Transient Response
3. RC Delay Model
   a. Effective Resistance
   b. Gate and Diffusion Capacitance
   c. Elmore Delay

**Chapter 5 – Power**
1. Dynamic
a. Activity Factor
b. Capacitance
c. Voltage
d. Frequency
e. Short-Circuit Current
f. Resonant Circuits

2. Static
   a. Sub-Threshold Leakage
   b. Gate Leakage
   c. Junction Leakage

Chapter 7 – Scaling
1. Transistor
2. Interconnect

Chapter 9 – Combinational Circuit Design
1. Circuit Families
   a. Static CMOS
   b. Pseudo-NMOS
   c. Dynamic Circuits
      i. Domino Logic
         1. Structure
         2. Keepers
         3. Charge-Sharing
   d. Pass-Transistor Circuits
2. Silicon-On-Insulator (SOI)
   a. Advantages and Disadvantages
   b. FINFET’s and Tri-Gate MOSFETS

Chapter 10 – Sequential Circuit Design
1. Sequencing Methods
   a. Setup and Hold Times
   b. Clock Borrowing
   c. Clock Skew
2. Circuit Design of Latches and Flip-Flops

Chapter 15 – Testing, Debugging, and Verification
1. Manufacturing Test Principles – Stuck-At Fault Model
2. Design for Testability
   a. AD-Hoc Testing
   b. Scan Design
   c. Built-In Self-Test (BIST)
   d. Boundary Scan