Engr433 Exam #1 - Review Sheet

This exam will be closed book and one hour in length. You may use one side of an $8^{1/2"}$x11" cheat sheet.

Combinational Circuits

I. Number Systems and Conversions – Binary, Decimal, Hexadecimal
II. Boolean Algebra – Laws, Minimization
III. Representation Forms - Truth Tables, Sum of Products (SOP), Product of Sums (POS)
IV. Karnaugh Maps
    A. Plotting
    B. Simplification
    C. Entered Variable Mapping
    D. Don't Cares
    E. Map Compression and Expansion
V. Combinational Circuits
    A. Multiplexers and Demultiplexers - Combinational Logic Design
    B. Decoders - Combinational Logic Design
    C. Other MSI Functions Like Encoders, Arithmetic Circuits, etc.

Sequential Circuits

I. Latch Types – D, Toggle, JK
II. Latch Design
    1. Basic Cell
    2. Function Table
    3. Excitation Table
III. Flip-Flops
    1. Types – D, JK, Toggle
IV. Synchronous Sequential Machines - General Models, State Diagrams
V. State Machine Design and Implementation
    1. General Models
    2. Alternative Architectures
VI. Other Synchronous Functions – Counters, Shift Registers, etc.

Programmable Logic

I. Standard Chips
II. Programmable Logic Arrays (PLA)
III. Programmable Array Logic (PAL)
IV. Complex Programmable Logic Devices (CPLD)
V. Field Programmable Gate Arrays (FPGA)
VI. Custom Integrated Circuit Design (IC)

Laboratory

I. Noise
II. Sequential Circuit Construction and Debugging
III. FPGA Implementation