Overview

- In this presentation we cover:
  - Registers, which store multiple bits;
  - Shift registers, which shift the contents of registers;
  - Counters of various types.
Review - Sequential Circuits

- **Combinational** – outputs depend only on the inputs;
- **Sequential** – output depends on input and past behavior:
  - Requires use of storage elements;
  - Content of the storage elements is called *state*;
  - Circuit goes through a sequence of states as a result of changes in inputs.
- **Synchronous** – Controlled by a clock;
- **Asynchronous** – No central clock.

Latches and Flip-Flops
Multibit Registers and Latches

74x374 8-bit Register
Shift Registers

A *shift register* is an n-bit register with a provision for shifting stored data by one bit position at each tick of the clock.

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Shift Registers – Serial-in, Parallel-out

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Engr354 - Registers and Counters
### 74x194 4-bit Universal Shift Register

<table>
<thead>
<tr>
<th>Function</th>
<th>S1</th>
<th>S0</th>
<th>QA&lt;sup&gt;0&lt;/sup&gt;</th>
<th>QB&lt;sup&gt;0&lt;/sup&gt;</th>
<th>QC&lt;sup&gt;0&lt;/sup&gt;</th>
<th>QD&lt;sup&gt;0&lt;/sup&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hold</td>
<td>0</td>
<td>0</td>
<td>QA</td>
<td>QB</td>
<td>QC</td>
<td>QD</td>
</tr>
<tr>
<td>Shift right</td>
<td>0</td>
<td>1</td>
<td>RIN</td>
<td>QA</td>
<td>QB</td>
<td>QC</td>
</tr>
<tr>
<td>Shift left</td>
<td>1</td>
<td>0</td>
<td>QB</td>
<td>QC</td>
<td>QD</td>
<td>LIN</td>
</tr>
<tr>
<td>Load</td>
<td>1</td>
<td>1</td>
<td>A</td>
<td>B</td>
<td>C</td>
<td>D</td>
</tr>
</tbody>
</table>

Table 8-24
Function table for the 74×194 4-bit universal shift register.

![Logic diagram](image)

Figure 8-41
Logic diagram for the 74×194 4-bit universal shift register, including pin numbers for a standard 16-pin dual in-line package.
**74x194 4-bit Universal Shift Register**

Figure 8-42

Simplest design for a 4-bit, 4-state ring counter with a single circulating 1.

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**74x194 4-bit Universal Shift Register**

Figure 8-43

Timing diagram for a 4-bit ring counter.
Counters

- **Counter** – generally used for any clocked sequential circuit whose state diagram contains a single cycle;
- **Modulus** – the number of states in the cycle;
- A counter with m states is called a modulus-\(m\) counter or a divide-by-\(m\) counter;
- **Ripple** counters (rare due to delays);
- **Synchronous** counters (common):
  - Connects all of its flip-flop clock inputs to the same common \(CLK\) signal so that all flip-flop outputs change at the same time.

Synchronous 4-bit Binary Counter – 74x163

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Current State</th>
<th>Next State</th>
</tr>
</thead>
<tbody>
<tr>
<td>(CL), (LD), (ENT), (EMP)</td>
<td>(Q0)</td>
<td>(Q0)</td>
</tr>
<tr>
<td>(Q1)</td>
<td>(Q1)</td>
<td>(Q1)</td>
</tr>
<tr>
<td>(Q2)</td>
<td>(Q2)</td>
<td>(Q2)</td>
</tr>
<tr>
<td>(Q3)</td>
<td>(Q3)</td>
<td>(Q3)</td>
</tr>
</tbody>
</table>

Table 8-13
State table for a 74x163 4-bit binary counter.
**Synchronous 4-bit Binary Counter – 74x163**

Figure 8-28
Logic diagram for the 74x163 synchronous 4-bit binary counter, including pin numbers for a standard 16-pin DIP package.

**Synchronous 4-bit Binary Counter – 74x163**

Figure 8-29
Connections for the 74x163 to operate in a free-running mode.
Synchronous 4-bit Binary Counter – 74x169

![Logic symbol for the 74x169 updown counter.]

Ring Counter

(a) An \( n \)-bit ring counter

(b) A four-bit ring counter
Johnson Counter

(a) Circuit

(b) Timing diagram

Three-Bit Up-Counter

(a) Circuit

(b) Timing diagram
Three-bit Down-Counter

(a) Circuit

(b) Timing diagram

Four-bit Synchronous Up-Counter

(a) Circuit

(b) Timing diagram
Inclusion of Enable and Clear Capability

Modulo-6 Counter with Synchronous Reset
Modulo-6 Counter with Asynchronous Reset

(a) Circuit

(b) Timing diagram

A Two-digit BCD Counter
Summary

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