Engr433: Digital Design

Implementation Technologies

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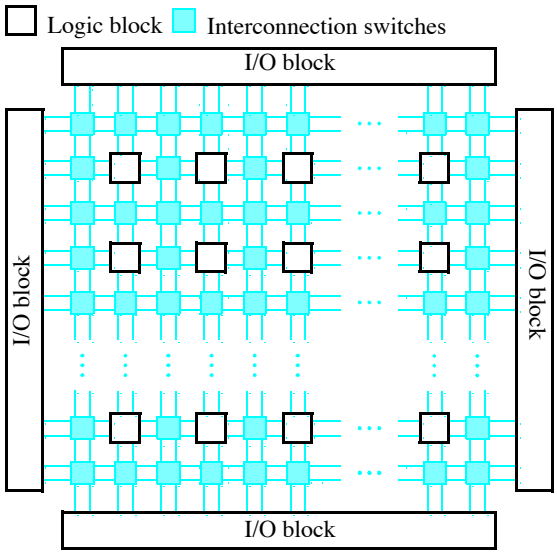
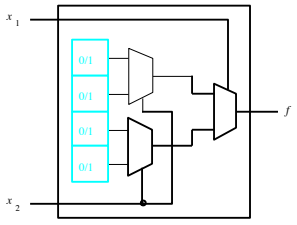
Implementation Overview

- How digital circuits are implemented
  - Standard chips;
  - Programmable logic;
    - Programmable logic array (PLA);
    - Programmable array logic (PAL);
    - Complex programmable logic devices (CPLD);
    - Standard cells;
    - Field programmable gate arrays (FPGA).
  - Custom chips.

Structure of an FPGA



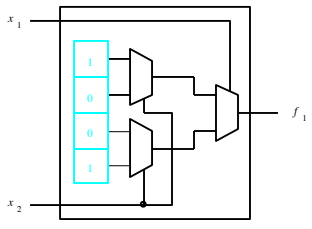
Combinational Logic Blocks - Lookup Tables



(a) Circuit for a two-input LUT

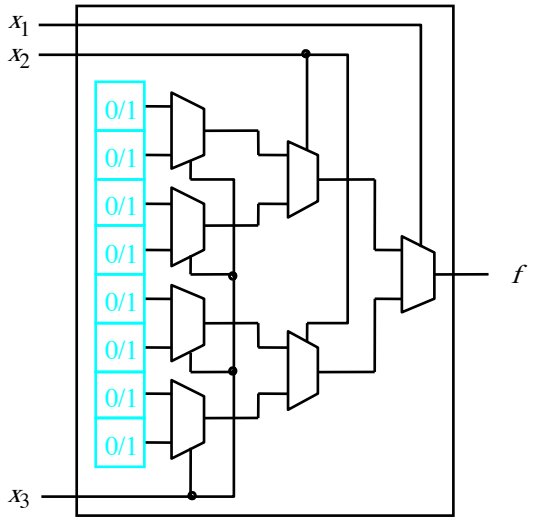
x_1	x_2	f_1
0	0	1
0	1	0
1	0	0
1	1	1

(b) $f_1 = \bar{x}_1 \bar{x}_2 + x_1 x_2$

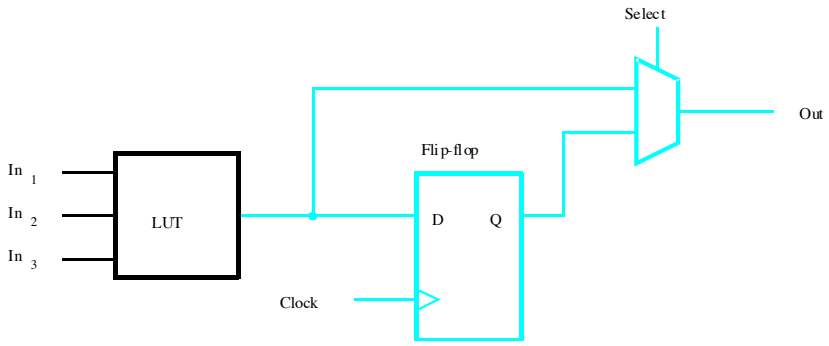


(c) Storage cell contents in the LUT

A Three-Input LUT



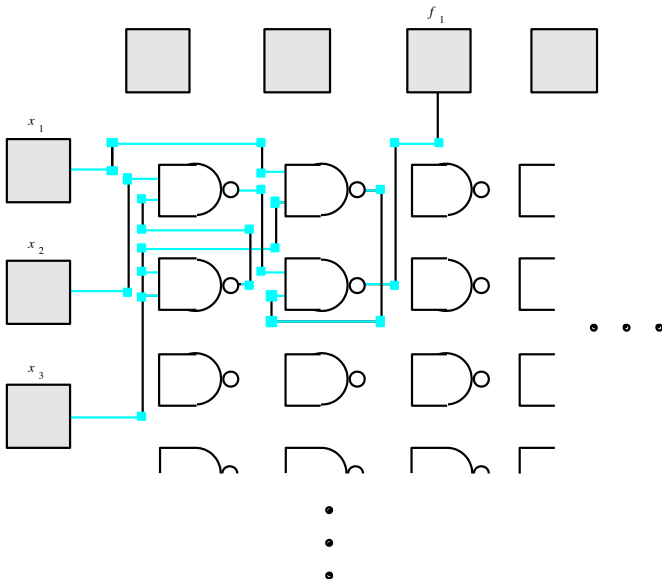
Inclusion of a Flip-Flop with a LUT



Standard-Cell Integrated Circuits

- Gates are prebuilt and stored in a library;
- The gates needed for a design are selected and placed, and wires are routed between them;
- Standard-cell chips are one form of *application specific integrated circuits* (ASIC's);
- CAD tools exist to place and route gates once a design has been synthesized.

Example of a Logic Function in a Gate Array



Custom Chips

- Created from scratch;
- Designer selects number, placement, and connections for each and every transistor;
- Most dense and highest speed;
- Requires a substantial design effort;
- Used only when high performance and density (and maybe secrecy) is required
  - Like processors or memories.

Simulation

- A *functional simulator* is used to determine if a designed circuit operates correctly from a **logic** perspective;
- Circuit **verification:**
  - User provides input values to the circuit;
  - Simulator determines the circuit response;
  - User checks responses against desired outputs;
- A *timing simulator* is used to check correctness by incorporating the ***electrical*** characteristics of a logic design in addition to the *logical* performance. This simulation requires:
  - Technology mapping;
  - Layout synthesis.