# Engr433 Lab #2

## Sequential Circuit Design

**Name** _____

**Partner** _____ **Grade** _____/10

### Objectives

- Gain sequential logic design experience;
- Gain experience using a logic simulator (Logisim);
- Gain maturity in the construction and debugging of logic circuits.

### Circuit Components Required

- Various SSI and MSI IC's.
- Breadboards;
- Wire;
- Instruments as necessary.

### Procedure

- Design a 2-bit grey code counter that counts up if the one input **up/down** is asserted, otherwise it counts down. There are two outputs, X and Y. X is asserted when the present state has an odd number of bits asserted. Y is asserted when the present state bits are the same.
  - Use rising edge-triggered D flip-flops as your memory elements.
  - Simulate your design in Logisim.
  - Fully document your design following the 9-step design process presented in class.
  - Find an ***absolute minimum number of IC's needed to implement your design***.

- Wire up your circuit using the breadboards in the digital lab. Set $V_{dd}$ = 3.0 volts. Have your circuit checked out by the lab assistant before you leave lab. Here is a list of parts available for you to use:

| | |
|---|---|
| 74HC00 Quad 2-Input NAND Gate | 74HC74 Dual D Flip-Flop |
| 74HC02 Quad 2-Input NOR Gate | 74HC86 Quad 2-Input XOR Gate |
| 74HC04 Hex Inverter | 74HC138 3-to-8 Decoder |
| 74HC10 Triple 3-Input NAND Gate | 74HC139 Dual 2-to-4 Decoder |
| 74HC20 Dual 4-input NAND Gate | 74HC151 8-to-1 Multiplexer (maybe) |
| 74HC27 Triple 3-Input NOR Gate | 74HC153 Dual 4-to-1 Multiplexer |

### To Turn In

- Staple together
  - This handout;
  - A schematic of your circuit. This can be hand written if it is neat;
  - A hard copy of your simulation results. Make sure you have sufficient resolution on all traces;
  - A short write-up explaining your design, procedures, results, conclusions, and lessons learned. ***Each person*** must turn in a report;
  - This hard-copy information is due by the beginning of class on Wednesday, October 2.