Engr433 Homework #6

Digital Systems Design

Due: Tuesday, October 22, Start of Lab

Problem Definition

A timer is needed to measure the time between a first and second pressing of a push button activated by a person's finger. Time is to be counted in 100^{ths} of seconds up to 99 seconds. Switch bounce occurring in the first 10 milliseconds after the button is pressed should be ignored. If the time between first button press and second button press is equal to or greater than 5 seconds, the error light (LED16) should come on and remain on until the reset button is pressed. When a proper time interval has been measured, i.e. one that is less than 5 seconds, the number of 10^{ths} of a second will be displayed using 8 LEDs in BCD (binary coded decimal) notation. Pressing reset will initiate a new measurement.

References

- Xilinx documents on the class web page
  - *Schematic entry using Xilinx tools tutorial*
  - *Xilinx schematic library reference manual for ISE 14.7*
  - *Constraints file*

Design Flow

- Confirm your understanding of the problem and partition the design into subsystems;
- Create a block diagram;
- Create a fully documented state diagram;
- Create logic functions for the next-state and output logic;
- From the Xilinx library, find components and understand their operation.
- Enter your schematic design using the Xilinx schematic editor.

Input/Output Requirements

- sw8 will be the button that the user presses twice;
- sw16 will be the reset switch;
- led3 down to led0 will be the right-hand digit of the measured time;
- led7 down to led4 will be the left-hand digit of the measured time;
- led16 will be the error light indicating more than 5 seconds between presses of sw8;
- A 50 MHz clock oscillator is available on pin T9 on the WWU spartan6 boards and named *mclk* in the constraints file.

Notes

- Refer to the *constraints file* on the course web page that indicates what the input/output pin names are and enter these accordingly on your schematic.
- The Xilinx library for schematic driven design contains D flip-flops, D latches, counters, many types of AND, OR, NAND, NOR, XOR gates with various numbers of inputs, 2:1 mux, 4:1 mux, 8:1 mux, 2:4 decoder, 3:8 decoder, etc.

Approach

Create a block diagram showing the functional blocks you believe will be needed (functional blocks could include state machines, counters, clock generators, displays, etc.). After creating a block diagram, if a state machine is needed, design the next-state logic for that state machine.

To Turn In

- Nothing. But … your grade on this homework assignment will be given to you in the first 15 minutes of lab time on Tuesday, October 22 based on the completeness of your design and how much has been entered into the Xilinx schematic editor.