Engr433 Homework #5

Sequential Review – Part IV

Due: Tuesday, October 8, Start of Lab

State Machine Design

For the following state diagram, design a state machine following these guidelines:

- Use any state machine architecture that you wish including Mealy or Moore, state decoder, direct addressed multiplexer, etc., or any combination;
- Use rising edge-triggered D flip-flops as your storage elements;
- Simulate if you wish, but it is not required;
- Minimize the number of IC's needed to implement youir design and state how many that would be;
- Your solution should include state diagrams, minimized equations, and a schematic (can be hand-drawn if very neat);
- Work with your lab partner if at all possible.