Engr433 Homework #4

Sequential Review – Part III

Due: Monday, October 4, Start of Class

State Machine Design

For the following problem, follow these guidelines:

- Use rising edge-triggered flip-flops as your storage elements;
- Simulate if you wish, but it is not required;
- Feel free to follow the state-machine design process outlined in class;
- Minimize the number of IC's needed to implement youir design and state how many that would be for each case;
- Your solutions should include state diagrams, minimized equations, and a schematic (can be hand-drawn if very neat).

Design a state machine that counts either up or down (depending on an **up/down** input) through a 3-bit grey-code sequence:

$$000 \rightarrow 001 \rightarrow 011 \rightarrow 010 \rightarrow 110 \rightarrow 111 \rightarrow 101 \rightarrow 100$$

There are two outputs, P and Q. P is asserted when the present state has two or more bits asserted, except for the 011 state where P is not asserted. Q is asserted when present states A and B are different (A being the MSB). Repeat your design using the alternative architectures listed below:

- A direct addressed mux;
- An indirect addressed mux.