Engr433 Homework #2

Sequential Review

Due: Wednesday, October 2, Start of Class

State Machine Design

For the following 2 problems, follow these guidelines:

- Use rising edge-triggered flip-flops as your storage elements;
- Simulate if you wish, but it is not required;
- Feel free to follow the state-machine design process outlined in class;
- Minimize the number of IC's needed to implement youir design and state how many that would be;
- Your solutions should include state diagrams, minimized equations, and a schematic (can be hand-drawn if very neat).

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1. Design a sequential circuit that will perform according to the following specifications: Starting from an initial state of A, this circuit will sample an input line, START, and remain in this state until the START signal becomes ASSERTED. Upon the first rising edge which senses the START condition, this circuit is to cycle from state A to State B to State C on successive rising edges of the clock. Once in state C, the START line is again sampled. It the START signal remains ASSERTED, the machine is to remain in state C generating an output, CONT, until the NOT_ASSERTED condition of START is sensed by the machine at which time it is to move to state D, generate another output, DONE, then move back to state A.

2. Design a state machine that implements the following sequence and repeats indefinately:

   $00 \rightarrow 10 \rightarrow 00 \rightarrow 11$