Engr433   Homework #1

Combinational Review

Due: Friday, September 27, Start of Class

Conventional K-maps

1. Use conventional K-maps to find a minimal sum-of-products expression for the following logic functions:

   a) $F(a,b,c) = \text{minterms}(1,3,5,6,7)$

   b) $G(a,b,c,d) = \text{minterms}(1,2,3,4,5,6,7,9,10,11,13)$.

2. Derive a minimum algebraic expression for the function $f(a,b,c,d) = \text{minterms}(4,8,11,13) + D(2,12,15)$ where D represents the don't care condition.

Entered Variable Map Compression

1. Compress the function $f(a,b,c,d) = \Sigma m(0,1,2,3,5,8,12,13,14)$ into a 3-variable map with d as the map-entered variable.

2. Compress the function $f(a,b,c,d) = \Sigma m(0,1,2,3,5,8,12,13,14)$ into a 2-variable map with a and c as the map-entered variables.

Entered Variable Minimization

1. Compress the K-map shown below into a three-variable K-map with *A* as the entered variable. Simplify each cell as far as possible. Place your answer in the K-map provided. Do not assume values for the don't care cells.

AB \ CD	00	01	11	10
00	Ø	1	Ø	1
01	1	0	0	0
11	0	0	1	1
10	Ø	1	1	Ø

D \ BC	00	01	11	10
0				
1				

2. Extract minimum SOP cover from either map above.

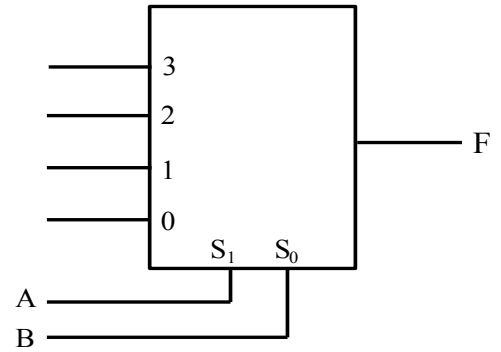3. Expand the K-map shown below into the four-variable K-map shown on the right.

B \ CD	00	01	11	10
0	A	1	A	$(\overline{A}) + A$
1	1	Ø	$\overline{A}$	0

| AB \ CD	00	01	11	10
00				
01				
11				
10				

Combinational Design

1. Implement the following logic function with a 4 to 1 multiplexer and minimum logic gates (if necessary). Make all inputs and outputs asserted high. Show proper connections to the symbol below.

$$F(A, B, C) = \sum m(1,2,4,7)$$

2. Implement the same function shown above using a 2 to 1 multiplexer and minimum logic gates (if necessary). Again, make all inputs and outputs asserted high. Show the proper connections to the symbol below.
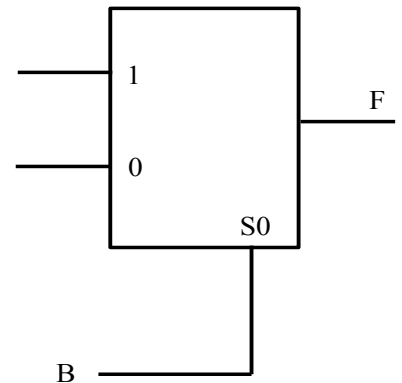
Combinational Analysis

Fill in the table below for the circuit at the right. Consider B to be the most significant select bit for the multiplexer. The FA in the circuit means *Full Adder*. (Hint: express inputs to the MUX in equation form).
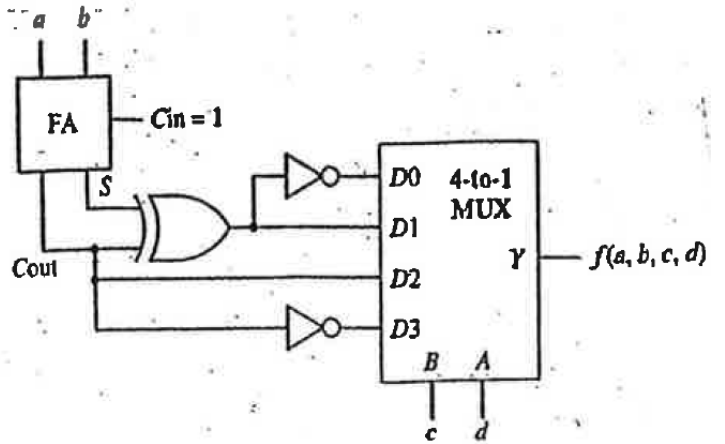
a	b	c	d	f(a,b,c,d)
0	0	0	1	
0	1	0	1	
1	0	0	1	
1	1	0	1	
0	0	1	0	
0	1	1	0	
1	0	1	0	
1	1	1	0	

Circuit Simulation

1. Using the circuit below, construct a truth table listing the inputs on the left and the output on the right.
2. Download and install the Logisim circuit simulator (link on course web page) onto your own personal computer.
3. Simulate all combinations of inputs in the circuit below and verify your truth table from step 1 above.