Inter-Integrated Circuit (I\textsuperscript{2}C) Serial Communication Protocol

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Parallel Communication

\[ \mu\text{P} \quad D0 \quad D7 \quad \text{Mem} \]
Parallel Communication

- Microprocessor (μP)
- Memory (Mem)
- Data lines (D0, D1, D2, D3, D4, D5, D6, D7)
- Clock (CLK)
- Address lines (A0, A1, A2, A3, A4, A5, A6, A7)
Parallel Communication

µP
• D0
• D7
• A0
• A
• A7
• READ
• WRITE
• CLK

• Me
• D7
• READ
• WRITE
• CLK
• ENAB
• LE

Parallel Communication
Parallel Communication

Data Bus

c0
c1
c2
c3
c4
c5
c6
c7

Address Bus

c0
a0
a1
a2
a3
a4
a5
a6
a7

Parallel Communication

clk

addr

0x88

data

0xAA

Read

Write

Enable
Serial Communication – I²C

Serial Communication – One Wire
The I2C Bus

- Inter-Integrated-Circuit or I2C (pronounced I-too-see or I-squared-see) is a synchronous serial protocol that uses a bi-directional data line and supports multiple slave devices controlled by a I2C bus master.
- The clock line is called SCL, the data line SDA.
I2C bus

- Invented by Philips in the early 1980s
  - The division is now NXP
  - Was a patented protocol, but patent has expired
  - NXP issues hard addresses to manufacturers of I2C devices
- Originally used by Philips inside television sets
- Now a very common peripheral bus standard
- Intended for use in embedded systems
- Also used in PCs as a variant to the SMBus (System Management Bus)

I2C Overview

- I2C consists of two bidirectional bus lines
  - Serial data signal (SDA)
  - Serial clock signal (SCL)
  - Multi-master architecture
  - Open collector bus driver
  - Pull-up resistors
- Transmit and Receive Operations
- 7- and 10-bit Addressing Modes
- Unrestricted number of data bytes transmitted per transfer
- Multi-Master, Master, or Slave configurations
What is I²C?

• A Small Area Network connecting ICs and other electronic systems
• Originally intended for operation on one single board / PCB
  – Synchronous Serial Signal
  – Two wires carry information between a number of devices
  – One wire used for the data
  – One wire used for the clock
• Today, a variety of devices are available with I²C Interfaces
  – Microcontroller, EEPROM, Real-Timer, interface chips, LCD driver, A/D converter

What is I²C used for?

• Data transfer between ICs and systems at relatively low rates
  – “Classic” I²C is rated to 100K bits/second
  – “Fast Mode” devices support up to 400K bits/second
  – A “High Speed Mode” is defined for operation up to 3.4M bits/second
• Reduces Board Space and Cost By:
  – Allowing use of ICs with fewer pins and smaller packages
  – Greatly reducing interconnect complexity
I2C START and STOP Operations

- A START sequence begins a bus transmission by transitioning SDA from High to Low while SCL is High.
- A STOP sequence ends a transmission. The Stop sequence occurs when the master brings SDA from Low to High while SCL is High.

I2C Operation

- The I2C bus master generates SCL and initiates communication with one of the slave devices. Each device has a unique address for device selection.
- A device address can be a combination of bits that are “hard-wired” into the chip design and one or more pins on the device. These pins can be wired High or Low to select an address that doesn't conflict with other devices on the I2C bus.
- Pull-up resistors are required on both the clock and data lines.
SDA Signal

- All addresses, data and acknowledge signals are sent over the SDA line, most-significant bit first.
- When transmitting data or acknowledging read data from the slave, the SDA signal changes in the middle of the low period of SCL and is sampled in the middle of the high period of SCL.
- 2000 ohm pull-up resistor needed for proper operation.

SCL Signal

- SCL is the common clock for the I2C Controller.
- Not a “traditional” clock.
- Normally is kept “high” using a pull-up resistor.
- Pulsed by the master during data transmission.
- During the high period of the clock, the slave pulls the SCL signal Low to suspend the transaction. When the slave has released the line, the I2C Controller continues the transaction.
- 2000 ohm pull-up resistor needed for proper operation.
I2C Data Transmission

- For a write, master transmits, slave acknowledges
- For a read, slave transmits, master acknowledges
- Transmission continues
  - Subsequent bytes sent
  - Continue until master creates stop condition

![Diagram of I2C data transmission](Source: ATmega8 Handbook)

I2C Write Sequence

- A typical I2C bus sequence for writing to a slave:
  - Send a START sequence.
  - Send the I2C device address.
  - Send the data byte.
  - Optionally send additional data bytes (after repeating START).
  - Send the STOP sequence after all data bytes have been sent.
- The Slave responds by setting the ACK bit (Acknowledge).
I2C Read Sequence

- Reading an I2C Slave device usually begins by writing to it. You must tell the chip which internal register you want to read.
- I2C Read Sequence:
  - Send the START condition.
  - Send the device address.
  - Send the number of the register you want to read.
  - Send a repeated START condition.
  - Send the device address.
  - Read the data byte from the slave.
  - Send the STOP sequence.

I2C Read Example

- I2C Read example using device address 1100000 and reading register number 1.
I²C Bus Characteristics

- Includes electrical and timing specifications, and an associated bus protocol.
- Two wire serial data & control bus implemented with the serial data (SDA) and clock (SCL) lines.
  - For reliable operation, a third line is required: Common ground.
- Unique start and stop condition.
- Slave selection protocol uses a 7-Bit slave address.
  - The bus specification allows an extension to 10 bits.
- Bi-directional data transfer.
- Acknowledgement after each transferred byte.
- No fixed length of transfer.

I²C Bus Definitions

- Master:
  - Initiates a transfer by generating start and stop conditions.
  - Generates the clock.
  - Transmits the slave address.
  - Determines data transfer direction.
- Slave:
  - Responds only when addressed.
  - Timing is controlled by the clock line.
I²C Hardware Details

- Devices connected to the bus must have an open drain or open collector output for serial clock and data signal.
- The device must also be able to sense the logic level on these pins.
- All devices have a common ground reference.
- The serial clock and data lines are connected to Vdd through pull up resistors.

I²C Electrical Aspects

- I²C devices are wire AND'ed together.
- If any single node writes a zero, the entire line is zero.
I2C Bus Addressing

Pull-ups are needed

PIC

SCL
SDA

10 K

10 K

I2C Peripheral
(address = 0b mmmmm A2 A1 A0 R/W#)

‘0’ Master to Slave

‘1’ Slave to Master

External Connections
personalize address

SCL: Clock
SDA: Data
Both SCL, SDA
are bidirectional

FC Peripheral

SCL
A2
A1
A0

FC Peripheral

SCL
A2
A1
A0

No chip selects needed!!!!!