Engr354 **Mid-term #2** **Autumn, 2016**

NAME KEY SCORE _____/50

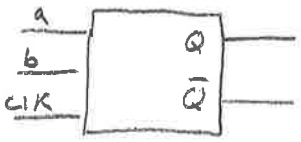
This is a closed book test except for one sheet of private reference.

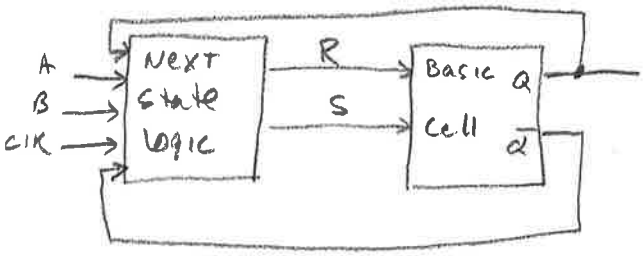
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16 ~~20~~ pts Latch Design

Design a latch that uses the combined version of the basic cell, as developed in class, as a storage element (excitation table shown below). This latch has two inputs **A** and **B**, in addition to a **clk** signal which acts as a gate. The output should set if A and B are 00, hold if A and B are 01, reset if A and B are 10, or toggle if A and B are 11(function table shown below). Create the following items in your design:

a. Block diagram showing inputs and outputs;
b. Truth table for the next state logic;
c. Minimized equations for the inputs to the basic cell;
d. Draw a schematic, make it readable not necessarily pretty.





A B	Action
0 0	Set
0 1	Hold
1 0	Reset
1 1	Toggle

$Q_n \rightarrow Q_{n+1}$	S R
0 0	0 Ø
0 1	1 0
1 0	0 1
1 1	Ø 0

CLK A B Q_N	Q_{N+1}	S R
0 0 0 0	0	0 Ø
0 0 0 1	1	Ø 0
0 0 1 0	0	0 Ø
0 0 1 1	1	Ø 0
0 1 0 0	0	0 Ø
0 1 0 1	1	Ø 0
0 1 1 0	0	Ø Ø
0 1 1 1	1	Ø 0
1 0 0 0	1	1 0
1 0 0 1	1	Ø 0
1 0 1 0	0	0 Ø
1 0 1 1	1	Ø 0
1 1 0 0	0	0 Ø
1 1 0 1	0	0 1
1 1 1 0	1	1 0
1 1 1 1	0	0 1

CLK A

BQ_N	00	01	11	10
00	0	0	0	1
01	Ø	Ø	0	Ø
11	Ø	Ø	0	Ø
10	0	0	1	0

$S = CLK \cdot \bar{A} \cdot \bar{B} + CLK \cdot A \cdot B \cdot \bar{Q_N}$

CLK A

BQ_N	00	01	11	10
00	Ø	Ø	Ø	0
01	0	0	1	0
11	0	0	1	0
10	Ø	Ø	0	Ø

$R = CLK \cdot A \cdot Q_N$

16

20 pts State Diagrams and State Machine Design

1 pts List the input(s). X, Y

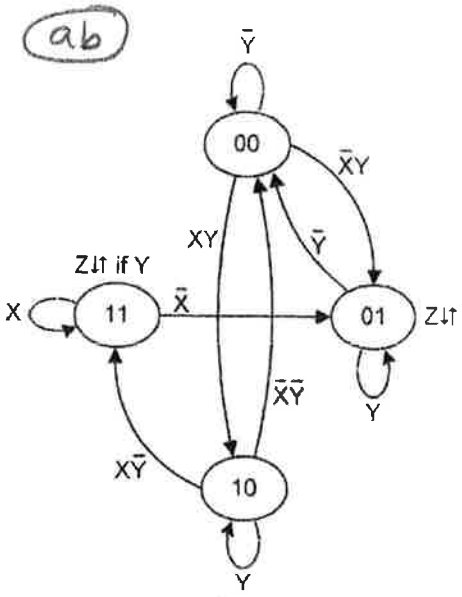
1 pts List the output(s). Z

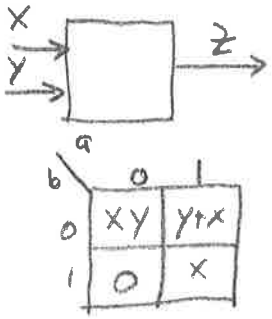
1 pts List the next states of the 11 state. 11, 01

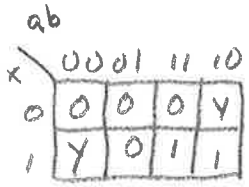
1 pts List the previous states of the 00 state. 00, 01, 10

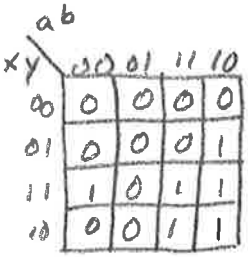
12 pts Using RET flip-flops, complete the following items:
- a. Block diagram showing inputs and outputs;
- b. Truth table or K-maps for the next state logic;
- c. Minimized equations for the next state logic;
- d. Minimized equations for the output logic;
- e. *You do not need to draw a schematic.*

ab

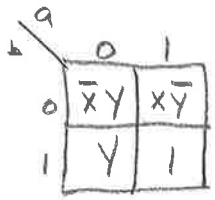


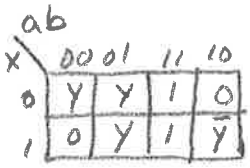


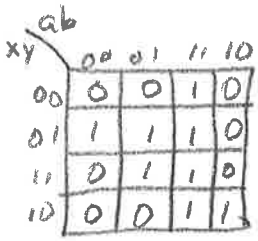




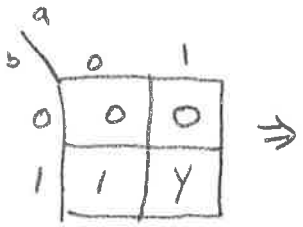
$d_a = ax + \bar{b}xy + a\bar{b}\bar{y}$

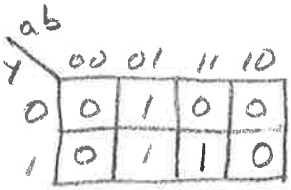






$d_b = ab + by + \bar{a}\bar{x}y + ax\bar{y}$





$Z = \bar{a}b + by$

9 pts Sequential Analysis

Complete the following timing diagram for signals Q_1 and Q_2 and determine the logic function of the block labeled *f*.

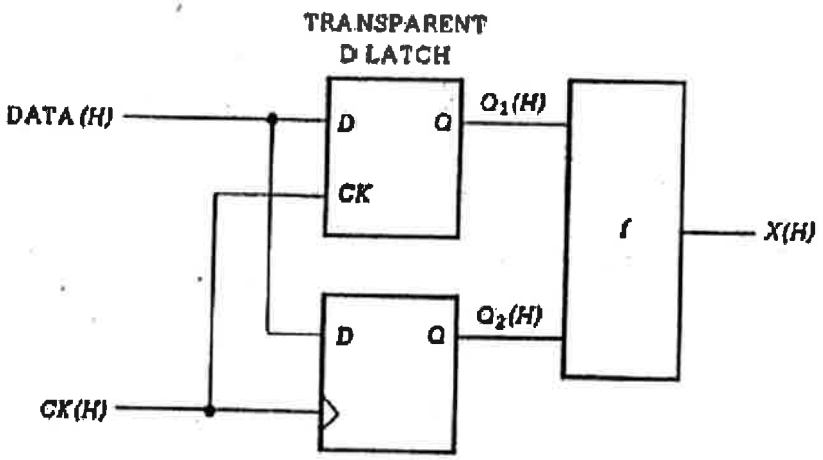
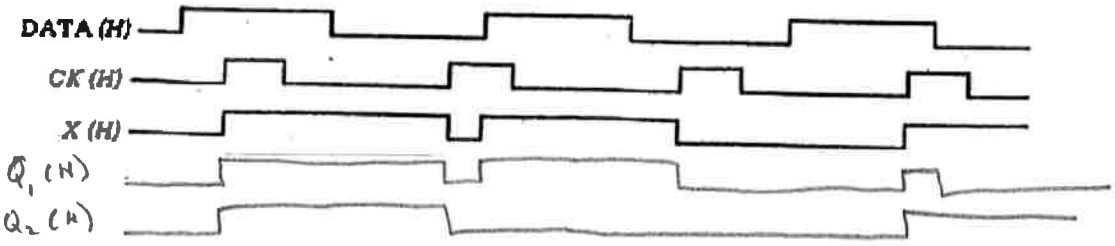


Fig. P5-2.



X(H) is high whenever Q_1 or Q_2 are high so

$X = Q_1 + Q_2$ f is an OR gate

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1 pt each True/False Questions. Circle the correct response.

T or (F) In *sequential* circuits, the outputs depends only on the inputs.

T or (F) In a sequential state machine, the *Present State* code can be found at the inputs to the flip-flops.

(T) or F In a synchronous state machine, you would find the *Next State* code at the memory inputs.

T or (F) A synchronous reset will reset the output of a flip-flop independent of the state of the clock signal.

5 pts State Machine Analysis (Stretch the mind problem!)

Create a fully-labelled state diagram from the circuit below.

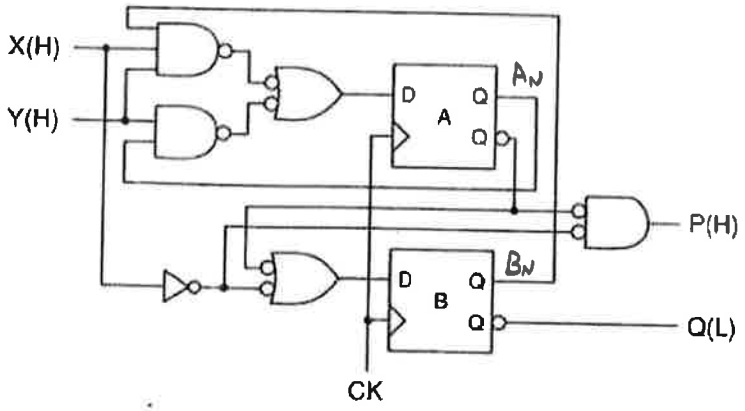
1) FIND equation for the output P.

$P = AX$

2) FIND equations for next state codes

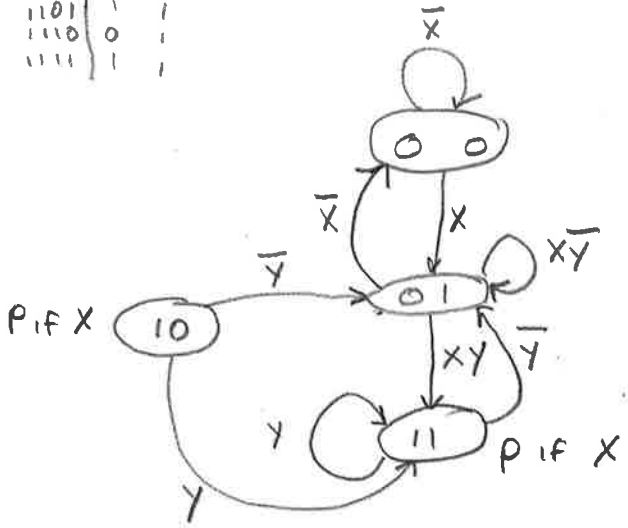
$a_{n+1} = Bxy + yA$

$b_{n+1} = X + A$



3) truth table

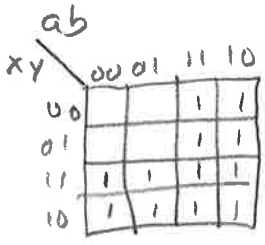
a b x y	a_{n+1}	b_{n+1}
0 0 0 0	0	0
0 0 0 1	0	0
0 0 1 0	0	1
0 0 1 1	0	1
0 1 0 0	0	0
0 1 0 1	0	0
0 1 1 0	0	1
0 1 1 1	1	1
1 0 0 0	0	1
1 0 0 1	1	1
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1 1 0 1	1	1
1 1 1 0	0	1
1 1 1 1	1	1



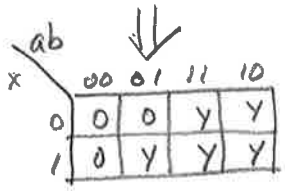
3a) K maps



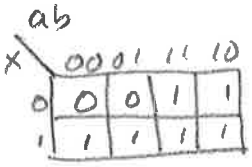
$a_{n+1} = Ay + bxy$

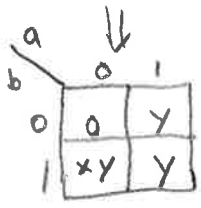


$b_{n+1} = A + X$

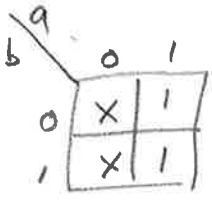


a_{n+1}





a_{n+1}



b_{n+1}