Engr354 Final Exam Review Sheet

The final exam will be closed book and 2 hours in length. Resources you may use during the exam are your calculator and up to three cheat sheets ($8^{1/2}$"x11"). The final exam will be comprehensive.

I. Number Systems
  A. Types
    1. Binary
    2. Decimal
    3. Hexadecimal
II. Boolean Algebra
  A. Laws
    1. Not, And, Or
    2. Commutative, Associative, Distributive
    3. Absorptive, Consensus
    4. DeMorgan's
  B. Minimization
III. Representation Forms
  A. Truth Tables
  B. Canonical
  C. Sum of Products (SOP)
    1. Minterms
  D. Product of Sums (POS)
    1. Maxterms
IV. Karnaugh Maps
  A. Plotting
  B. Simplification
  C. Entered Variable Maps (EVMs)
  D. Incompletely Specified Functions (don't cares)
  E. Map Compression and Expansion
V. Combinational Circuits
  A. Decoders
    1. Combinational Logic Design
  B. Multiplexers and Demultiplexers
    1. Combinational Logic Design

I. Combinational Circuits
  E. Arithmetic Circuits
    1. Adders
      a. Half
      b. Full
      c. Ripple-Carry Adders
      d. Carry Look-Ahead Adders
II. Sequential Circuits
  A. Latches
    1. Basic Cell

a. Set Dominant
b. Reset Dominant
c. Function Table
d. Excitation Table

2. Latch Types
a. D
b. Toggle
c. JK

3. Latch Design

B. Flip-Flops
1. Clock types
a. Master-slave
b. Edge-triggered

2. Types
a. D
b. JK
c. Toggle

C. Synchronous Sequential Machines
1. General Models
2. State Diagram
3. Timing Diagram

D. State Machine Design
1. D Flip-flop
2. JK Flip-flop

III. Circuit Construction and Debugging

I. State Machine Design and Implementation
A. D
B. JK
C. Alternative Architectures

II. Counters and Shift Registers

III. Programmable Logic
A. Standard Chips
B. Programmable Logic Arrays (PLA)
C. Programmable Array Logic (PAL)
D. Complex Programmable Logic Devices (CPLD)
E. Field Programmable Gate Arrays (FPGA)
F. Custom Integrated Circuit Design (IC)

IV. Asynchronous Circuits

V. Project