

This will be a closed book test. One sheet of private reference and writing instruments are allowed, nothing else.

- I. Sequential Circuits
 - A. Latches
 - 1. Basic Cell
 - a. Set Dominant
 - b. Reset Dominant
 - c. Combined Form
 - d. Function Table
 - e. Excitation Table
 - 2. Latch Types
 - a. D
 - b. Toggle
 - c. JK
 - 3. Latch Design
 - B. Flip-Flops
 - 1. Clock types
 - a. Level-sensitive
 - b. Edge-triggered
 - 2. Types
 - a. D
 - b. JK
 - c. Toggle
 - C. Synchronous Machines
 - 1. State Diagram
 - 2. Timing Diagram
 - 3. Models
 - a. Moore Model
 - b. Mealy Model (allows conditional outputs)
 - D. State Machine Design
 - 1. D Flip-flops
 - 2. Alternative Architectures
 - a. State Decoder
 - b. Direct-addressed Multiplexer
 - c. Indirect-addressed Multiplexer
 - E. Counters and Shift Registers
- II. Circuit Construction and Debugging