Engr354: Digital Logic Circuits

Chapter 3: Implementation Technology

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Chapter 3 Overview

In this chapter you will learn about:
• How transistors are used as switches;
• Integrated circuit technology;
• Complementary Metal-Oxide-Semiconductor (MOS) logic gates;
• Programmable Logic Devices.
**Voltage Logic Levels**

- **$V_{DD}$**
- **$V_{L\text{ow}}$**
- **$V_{\text{low}}$**
- **$V_{SS}$** (Gnd)

**Voltage Waveforms**

- **$V_{DD}$**
- **$V_{A}$**
- **$Gnd$**

The diagrams illustrate the voltage logic levels and waveforms relevant to digital electronics, emphasizing the transitions and propagation delays.
Transistors as Switches

(a) A simple switch controlled by the input $x$

(b) NMOS transistor

(c) Simplified symbol for an NMOS transistor

Figure 3.2. NMOS transistor as a switch.

NMOS and PMOS Transistors

(a) NMOS transistor

(b) PMOS transistor

Figure 3.4. NMOS and PMOS transistors in logic circuits.
Physical Structure of an NMOS Transistor

Structure of a CMOS Circuit
CMOS Realization of a NOT Gate

(a) Circuit

(b) Truth table and transistor states

\[
\begin{array}{c|cc|c}
 x & T_1 & T_2 & f \\
 0 & \text{on} & \text{off} & 1 \\
 1 & \text{off} & \text{on} & 0 \\
\end{array}
\]

CMOS Realization of a 2-Input Nand Gate

(a) Circuit

(b) Truth table and transistor states

\[
\begin{array}{c|ccccc|c}
 x_1 & x_2 & T_1 & T_2 & T_3 & T_4 & f \\
 0 & 0 & \text{on} & \text{on} & \text{off} & \text{off} & 1 \\
 0 & 1 & \text{on} & \text{off} & \text{off} & \text{on} & 1 \\
 1 & 0 & \text{off} & \text{on} & \text{off} & \text{off} & 1 \\
 1 & 1 & \text{off} & \text{off} & \text{on} & \text{on} & 0 \\
\end{array}
\]
Programmable Logic Overview

- How digital circuits are implemented
  - Standard chips;
  - Programmable logic;
    • Programmable logic array (PLA);
    • Programmable array logic (PAL);
    • Complex programmable logic devices (CPLD);
    • Standard cells;
    • Field programmable gate arrays (FPGA).
  - Custom chips.

Standard Chips

(a) Dual-inline package

(b) Structure of 74HC04 chip
Implementation of \( f = x_1x_2 + x_2x_3 \)

Programmable Logic Device as a Black Box
Structure of a Programmable Logic Array (PLA)

Input buffers and inverters

AND plane

OR plane

Gate-Level Diagram of a PLA
Example Schematic of a PLA

PLA and PAL Characteristics

- Programmable OR and AND planes
  - Hard to fabricate correctly;
  - Reduced speed performance.
- Led to the development of Programmable Array Logic (PAL)
  - AND plane programmable, OR plane fixed;
  - Simpler to manufacture, less expensive, better performance.
An Example of a PAL

Two Function PAL
PLD Output Logic

- GAL – Generic Array Logic

Figure 8.17
Output logic macrocells for the 16V8R: (a) combinational; (b) registered.

Logic Diagram of the PAL16L8
A PLD Programming Unit

Plastic Leaded Chip Carrier (PLCC) and Socket
Pin Grid Array (PGA) Package

(b) Pin grid array (PGA) package (bottom view)

Complex Programmable Logic Device (CPLD)
CPLD Packaging and Programming

(a) CPLD in a Quad Flat Pack (QFP) package

(b) JTAG programming

Field Programmable Gate Arrays (FPGA)

- Programmable logic presented so far is good for small circuits
  - 74HC00 (series in general), a few to 10’s of gates;
  - PLA and PAL, a few hundred gate equivalents;
  - CPLD, a few thousand up to 25K gate equivalents.
- Need for larger programmable devices
- Enter FPGA’s
  - Do not contain AND and OR planes, rather logic blocks;
  - 10,000 up to 1,000,000 gate equivalents and more on the way.
Logic Blocks are Often Lookup Tables (LUT)

(a) Circuit for a two-input LUT

\[
\begin{array}{c|c|c}
  x_1 & x_2 & f_1 \\
  \hline
  0 & 0 & 1 \\
  0 & 1 & 0 \\
  1 & 0 & 0 \\
  1 & 1 & 1 \\
\end{array}
\]

\[ f_1 = x_1 \cdot x_2 + x_1 \cdot x_2 \]

(c) Storage cell contents in the LUT
A Three-Input LUT

Inclusion of a Flip-Flop with a LUT
Custom Chips

- Created from scratch;
- Designer selects number, placement, and connections for each and every transistor;
- Most dense and highest speed;
- Requires a substantial design effort;
- Used only when high performance and density (and maybe secrecy) is required
  - Like processors or memories.

Standard-Cell Chips

- Gates prebuilt and stored in a library;
- Gates needed for a design are selected and placed via synthesis algorithms, and wires are routed between them;
- Standard-cell chips are often called *application specific integrated circuits* (ASIC’s);
- CAD tools exist to place and route gates.
Gate-Arrays

- Parts of chip are prefabricated (transistors);
- Parts of chip are custom fabricated (wires);
- Provides cost savings since all template wafers are identical;
- Many variants exist.

Example of a Logic Function in a Gate Array
Programmable Logic Summary

• How digital circuits are implemented
  – Standard chips;
  – Programmable logic;
    • Programmable logic array (PLA);
    • Programmable array logic (PAL);
    • Complex programmable logic devices (CPLD);
    • Standard cells;
    • Field programmable gate arrays (FPGA);
    • Programming.
  – Custom chips.

Summary

In this chapter you learned about:
• How transistors are used as switches;
• Integrated circuit technology;
• Complementary Metal-Oxide-Semiconductor (MOS) logic gates;
• Programmable Logic Devices (PLD’s).