Digital Logic Homework #14

DUE: Friday, November 15

Objective

Learn state machine design using alternative architectures.

To Do

1) Using RET D flip-flops, design a state machine that counts either up or down (depending on an up/down input) through a 3-bit grey-code sequence:

$$000 \rightarrow 001 \rightarrow 011 \rightarrow 010 \rightarrow 110 \rightarrow 111 \rightarrow 101 \rightarrow 100$$

2) Repeat your design using the alternative architectures listed below:
   - A direct addressed mux;
   - An indirect addressed mux.

3) In all cases, compute the number of IC's needed to implement the design.

Turn In

- **Staple this assignment sheet** to your solutions, which are to be done in accordance with the school of engineering homework guidelines posted on the course web page.