Digital Logic          Homework #14

DUE:  Friday, November 15

Objective

Learn state machine design using alternative architectures.

To Do

1) Using RET D flip-flops, design a state machine that counts either up or down (depending on an up/down input) through a 3-bit grey-code sequence:

   000 → 001 → 011 → 010 → 110 → 111 → 101 → 100

2) Repeat your design using the alternative architectures listed below:
   • A direct addressed mux;
   • An indirect addressed mux.

3) In all cases, compute the number of IC’s needed to implement the design.

Turn In

• Staple this assignment sheet to your solutions, which are to be done in accordance with the school of engineering homework guidelines posted on the course web page.