Digital Logic

Homework #11

DUE:  Wednesday, November 9

Objective
To design a simple state machine.

To Do

• Using rising-edge-triggered (RET) D flip-flops, design a state machine that cycles indefinitely through the following sequence:

  00 → 10 → 11 → 01 and repeats.

• Wire it up and watch it work.
• Bring your circuit to class on the due date and demonstrate it to your friends.
• You may use a switch as the clock signal or the 1Hz clock signal provided on your logic boards.
• Be sure and tie the asynchronous preset and clear inputs high.

Turn In

• Staple this assignment sheet to your paper design, which is to be done in accordance with the school of engineering homework guidelines posted on the course web page.
• Notes on circuit construction, debugging, and operation.