**QUADRUPLLE 2-INPUT POSITIVE-NOR GATES**

- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 20-µA Max $I_{CC}$
- Typical $t_{pd} = 8$ ns
- ±4-mA Output Drive at 5 V
- Low Input Current of 1 µA Max

SN54HC02...J OR W PACKAGE
SN74HC02...D, DB, N, NS, OR PW PACKAGE

(TOP VIEW)

<table>
<thead>
<tr>
<th>Ta</th>
<th>Package</th>
<th>ORDERABLE PART NUMBER</th>
<th>TOP-SIDE MARKING</th>
</tr>
</thead>
<tbody>
<tr>
<td>PDIP – N</td>
<td>Tube of 25</td>
<td>SN74HC02N</td>
<td>SN74HC02N</td>
</tr>
<tr>
<td>SOIC – D</td>
<td>Tube of 50</td>
<td>SN74HC02D</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Reel of 2500</td>
<td>SN74HC02DR</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Reel of 250</td>
<td>SN74HC02DT</td>
<td></td>
</tr>
<tr>
<td>SOP – NS</td>
<td>Reel of 2000</td>
<td>SN74HC02NSR</td>
<td></td>
</tr>
<tr>
<td>SSOP – DB</td>
<td>Reel of 2000</td>
<td>SN74HC02DBR</td>
<td></td>
</tr>
<tr>
<td>TSSOP – PW</td>
<td>Tube of 90</td>
<td>SN74HC02PW</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Reel of 2000</td>
<td>SN74HC02PWR</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Reel of 250</td>
<td>SN74HC02PWT</td>
<td></td>
</tr>
<tr>
<td>CDIP – J</td>
<td>Tube of 25</td>
<td>SNJ54HC02J</td>
<td>SNJ54HC02J</td>
</tr>
<tr>
<td>CFP – W</td>
<td>Tube of 150</td>
<td>SNJ54HC02W</td>
<td>SNJ54HC02W</td>
</tr>
<tr>
<td>LCCC – FK</td>
<td>Tube of 55</td>
<td>SNJ54HC02FK</td>
<td>SNJ54HC02FK</td>
</tr>
</tbody>
</table>

*Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.*

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FUNCTION TABLE
(each gate)

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>B</td>
</tr>
<tr>
<td>H</td>
<td>X</td>
</tr>
<tr>
<td>X</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
</tr>
</tbody>
</table>

logic diagram (positive logic)

![Logic Diagram](image)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

- Supply voltage range, $V_{CC}$: $-0.5 \text{ V to } 7 \text{ V}$
- Input clamp current, $I_{IK}$ ($V_I < 0 \text{ or } V_I > V_{CC}$) (see Note 1): $\pm 20 \text{ mA}$
- Output clamp current, $I_{OK}$ ($V_O < 0 \text{ or } V_O > V_{CC}$) (see Note 1): $\pm 20 \text{ mA}$
- Continuous output current, $I_O$ ($V_O = 0 \text{ to } V_{CC}$): $\pm 25 \text{ mA}$
- Continuous current through $V_{CC}$ or GND: $\pm 50 \text{ mA}$
- Package thermal impedance, $\theta_{JA}$ (see Note 2): D package: $86 \degree \text{C/W}$, DB package: $96 \degree \text{C/W}$, N package: $80 \degree \text{C/W}$, NS package: $76 \degree \text{C/W}$, PW package: $113 \degree \text{C/W}$
- Storage temperature range, $T_{stg}$: $-65 \degree \text{C to } 150 \degree \text{C}$

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

<table>
<thead>
<tr>
<th></th>
<th>SN54HC02</th>
<th>SN74HC02</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$ Supply voltage</td>
<td>MIN</td>
<td>NOM</td>
<td>MAX</td>
</tr>
<tr>
<td>$V_{IH}$ High-level input voltage</td>
<td>$V_{CC} = 2 \text{ V}$</td>
<td>1.5</td>
<td>1.5</td>
</tr>
<tr>
<td>$V_{IL}$ Low-level input voltage</td>
<td>$V_{CC} = 2 \text{ V}$</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>$V_I$ Input voltage</td>
<td>0</td>
<td>$V_{CC}$</td>
<td>0</td>
</tr>
<tr>
<td>$V_O$ Output voltage</td>
<td>0</td>
<td>$V_{CC}$</td>
<td>0</td>
</tr>
<tr>
<td>$\Delta t/\Delta v$ Input transition rise/fall time</td>
<td>$V_{CC} = 2 \text{ V}$</td>
<td>1000</td>
<td>1000</td>
</tr>
<tr>
<td>$V_{CC} = 4.5 \text{ V}$</td>
<td>500</td>
<td>500</td>
<td></td>
</tr>
<tr>
<td>$V_{CC} = 6 \text{ V}$</td>
<td>400</td>
<td>400</td>
<td></td>
</tr>
<tr>
<td>$T_A$ Operating free-air temperature</td>
<td>$-55$</td>
<td>125</td>
<td>$-40$</td>
</tr>
</tbody>
</table>

NOTE 3: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
### Electrical Characteristics

**PARAMETER** | **TEST CONDITIONS** | **V<sub>CC</sub>** | **T<sub>A = 25°C</sub>** | **SN54HC02** | **SN74HC02** | **UNIT**
--- | --- | --- | --- | --- | --- | ---
**<sup>Vo</sup>H** | V<sub>IL</sub> or V<sub>IL</sub> | 2 V | 1.9 | 1.998 | 1.9 | 1.9 | V
 | | 4.5 V | 4.4 | 4.499 | 4.4 | 4.4 | V
 | | 6 V | 5.9 | 5.999 | 5.9 | 5.9 | V
 | | I<sub>OH</sub> = –4 mA | 4.5 V | 3.98 | 4.3 | 3.7 | 3.84 | V
 | | I<sub>OH</sub> = –5.2 mA | 6 V | 5.48 | 5.8 | 5.2 | 5.34 | V
**<sup>Vo</sup>L** | V<sub>I</sub> = V<sub>IH</sub> or V<sub>IL</sub> | 2 V | 0.002 | 0.1 | 0.1 | 0.1 | V
 | | 4.5 V | 0.001 | 0.1 | 0.1 | 0.1 | V
 | | 6 V | 0.15 | 0.26 | 0.4 | 0.33 | V
 | | I<sub>OL</sub> = 4 mA | 4.5 V | 0.17 | 0.26 | 0.4 | 0.33 | V
 | | I<sub>OL</sub> = 5.2 mA | 6 V | 0.15 | 0.26 | 0.4 | 0.33 | V
**<sup>i</sup>I** | V<sub>IL</sub> = V<sub>CC</sub> or 0 | 6 V | ±0.1 | ±100 | ±1000 | ±1000 | nA
**I<sub>CC</sub>** | V<sub>I</sub> = V<sub>CC</sub> or 0, I<sub>O</sub> = 0 | 6 V | 2 | 40 | 20 | µA
**C<sub>i</sub>** | 2 V to 6 V | 3 | 10 | 10 | 10 | pF

**Switching Characteristics**

**PARAMETER** | **FROM (INPUT)** | **TO (OUTPUT)** | **V<sub>CC</sub>** | **T<sub>A = 25°C</sub>** | **SN54HC02** | **SN74HC02** | **UNIT**
--- | --- | --- | --- | --- | --- | --- | ---
**<sup>t</sup>pd** | A or B | Y | 2 V | 45 | 90 | 135 | 115 | ns
 | | | 4.5 V | 9 | 18 | 27 | 23 | ns
 | | | 6 V | 8 | 15 | 23 | 20 | ns
**<sup>t</sup>i** | Y | 2 V | 38 | 75 | 110 | 95 | ns
 | | | 4.5 V | 8 | 15 | 22 | 19 | ns
 | | | 6 V | 6 | 13 | 19 | 16 | ns

**Operating Characteristics, T<sub>A = 25°C</sub>**

**PARAMETER** | **TEST CONDITIONS** | **TYP** | **UNIT**
--- | --- | --- | ---
C<sub>pd</sub> | Power dissipation capacitance per gate | No load | 22 | pF
PARAMETER MEASUREMENT INFORMATION

VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES

VCC

Input

50%

90%

90%

50%

10%

0 V

In-Phase
Output

VCC

90%

50%

10%

90%

0 V

Out-of-Phase
Output

90%

50%

10%

50%

VOL

t r

t f

VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

Input

50%

50%

0 V

In-Phase
Output

90%

90%

t PHL

t PLH

VOL

VCC

t f

0 V

Out-of-Phase
Output

50%

50%

10%

90%

VOH

t r

VOL

t PHL

VOH

t PLH

NOTES:
A. \( C_L \) includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: \( PRR \leq 1 \text{ MHz} \), \( Z_O = 50 \text{ \( \Omega \)} \), \( t_r = 6 \text{ ns} \), \( t_f = 6 \text{ ns} \).
C. The outputs are measured one at a time with one input transition per measurement.
D. \( t_{PLH} \) and \( t_{PHL} \) are the same as \( t_{pd} \).

Figure 1. Load Circuit and Voltage Waveforms
CERAMIC DUAL IN-LINE PACKAGE

14 LEADS SHOWN

### PINS **

<table>
<thead>
<tr>
<th>DIM</th>
<th>14</th>
<th>16</th>
<th>18</th>
<th>20</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.300 (7.62) BSC</td>
<td>0.300 (7.62) BSC</td>
<td>0.300 (7.62) BSC</td>
<td>0.300 (7.62) BSC</td>
</tr>
<tr>
<td>B MAX</td>
<td>0.785 (19.94)</td>
<td>0.840 (21.34)</td>
<td>0.960 (24.38)</td>
<td>1.060 (26.92)</td>
</tr>
<tr>
<td>B MIN</td>
<td>——</td>
<td>——</td>
<td>——</td>
<td>——</td>
</tr>
<tr>
<td>C MAX</td>
<td>0.300 (7.62)</td>
<td>0.300 (7.62)</td>
<td>0.310 (7.87)</td>
<td>0.300 (7.62)</td>
</tr>
<tr>
<td>C MIN</td>
<td>0.245 (6.22)</td>
<td>0.245 (6.22)</td>
<td>0.220 (5.59)</td>
<td>0.245 (6.22)</td>
</tr>
</tbody>
</table>

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

4040083/F 03/03
NOTES:  
A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package can be hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only.  
E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB
FK (S-CQCC-N**)  
LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

<table>
<thead>
<tr>
<th>NO. OF TERMINALS **</th>
<th>A MIN</th>
<th>A MAX</th>
<th>B MIN</th>
<th>B MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>0.342 (8.69)</td>
<td>0.358 (9.09)</td>
<td>0.307 (7.80)</td>
<td>0.358 (9.09)</td>
</tr>
<tr>
<td>28</td>
<td>0.442 (11.23)</td>
<td>0.458 (11.63)</td>
<td>0.406 (10.31)</td>
<td>0.458 (11.63)</td>
</tr>
<tr>
<td>44</td>
<td>0.640 (16.26)</td>
<td>0.660 (16.76)</td>
<td>0.495 (12.58)</td>
<td>0.560 (14.22)</td>
</tr>
<tr>
<td>52</td>
<td>0.739 (18.78)</td>
<td>0.761 (19.32)</td>
<td>0.495 (12.58)</td>
<td>0.560 (14.22)</td>
</tr>
<tr>
<td>68</td>
<td>0.938 (23.83)</td>
<td>0.962 (24.43)</td>
<td>0.850 (21.6)</td>
<td>0.858 (21.8)</td>
</tr>
<tr>
<td>84</td>
<td>1.141 (28.99)</td>
<td>1.165 (29.59)</td>
<td>1.047 (26.6)</td>
<td>1.063 (27.0)</td>
</tr>
</tbody>
</table>

0.020 (0.51)  
0.010 (0.25)  
0.005 (0.13)  
0.003 (0.08)  
0.020 (0.51)  
0.010 (0.25)  
0.050 (1.27)  
0.045 (1.14)  
0.035 (0.89)  
0.030 (0.76)  
0.020 (0.51)  
0.010 (0.25)  
0.055 (1.40)  
0.045 (1.14)  
0.028 (0.71)  
0.022 (0.54)  
0.005 (0.13)  
0.003 (0.08)  
0.005 (0.13)  
0.003 (0.08)  
0.050 (1.27)  
0.045 (1.14)  
0.035 (0.89)  
0.030 (0.76)  
0.020 (0.51)  
0.010 (0.25)  
0.020 (0.51)  
0.010 (0.25)  
0.050 (1.27)  
0.045 (1.14)  
0.035 (0.89)  
0.030 (0.76)
MECHANICAL DATA

N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

<table>
<thead>
<tr>
<th>PINS **</th>
<th>14</th>
<th>16</th>
<th>18</th>
<th>20</th>
</tr>
</thead>
<tbody>
<tr>
<td>A MAX</td>
<td>0.775 (19.69)</td>
<td>0.775 (19.69)</td>
<td>0.920 (23.37)</td>
<td>1.060 (26.92)</td>
</tr>
<tr>
<td>A MIN</td>
<td>0.745 (18.92)</td>
<td>0.745 (18.92)</td>
<td>0.850 (21.59)</td>
<td>0.940 (23.88)</td>
</tr>
<tr>
<td>MS–001 VARIATION</td>
<td>AA</td>
<td>BB</td>
<td>AC</td>
<td>AD</td>
</tr>
</tbody>
</table>

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
D. Falls within JEDEC MS-012 variation AB.
MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.15.

DIM PINS ** | 14 | 16 | 20 | 24
--- | --- | --- | --- | ---
A MAX | 10,50 | 10,50 | 12,90 | 15,30
A MIN | 9,90 | 9,90 | 12,30 | 14,70

4040062/C 03/03
NOTES:  
A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion not to exceed 0.15.  
D. Falls within JEDEC MO-150
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.15.
D. Falls within JEDEC MO-153
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<th>Applications</th>
<th></th>
</tr>
</thead>
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<td>amplifier.ti.com</td>
<td>Audio</td>
</tr>
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</tr>
<tr>
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<td>interface.ti.com</td>
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<td>microcontroller.ti.com</td>
<td>Security</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Telephony</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Video &amp; Imaging</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Wireless</td>
</tr>
</tbody>
</table>

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