The exam will be closed book. Materials that you may use during the test are:

- Your calculator and both sides of an 8½ x 11” cheat sheet that you may put anything on that you wish. Suggestions include:
  o Lecture material from textbook chapter 5 and other assorted topical lectures;
  o Homework specific issues;
  o Content from project presentations.

- Chapter 5 – Memory hierarchy
  a. Caches
     1. Direct accessed
     2. Fully associative
     3. N-way set associative
     4. Performance issues
        a. Block size tradeoffs
        b. Types of misses
           1. Compulsory
           2. Capacity
           3. Conflict
        c. Write-back vs. write-thru
        d. Block replacement policy
        e. Multi-level caches
  b. Virtual memory
     1. Address translation
     2. Page tables
     3. Translation Lookaside Buffers (TLB’s)
- Simultaneous multi-threading
- Project presentations
  o Konrad McClure – Super NES Architecture
  o Kyle Malaguit – Playstation 3’s Cell Engine
  o Kaden Sukachevin – Nature Inspired Architectures
  o Andrew Nascimento – Apple A-Series Processors
  o Russell Palma –
  o Greg Birge – ATtiny – Lite Custom Processor Design
  o Gary Jessup – Aegis Processor Architecture
  o Mason Wilde – Sinclair ZX Spectrum Computer
  o Jaymes Sullivan – Hardware Accelerators
  o Khalil Llewellyn – Exynos Processor
  o Travis Stanger – SRAM Memory
  o Andrew Binder – Drive Technologies
  o Dominick Christensen – History of DDR SDRAM
  o Caleb Froelich – Development of Non-volatile Memory
  o Caleb Herbel – Overview of Raid Technology
  o Daniel Arlt – Quantum Computing
  o Chrisner Garcesa – Quantum Computing
  o Elizabeth Ventura – Siri Architecture
  o Jeffrey Grange – GPU Architectures
  o Lucas Saca – GPU Architectures
  o Tanek Russell – Cloud Computing
  o Caleb Jurgensen – Custom Assembler Design
  o Lucas Marcondes – Web GUI Software Architecture
  o Phong Pham / Christian Terrado – Custom Booth Processor