Sandy Bridge Microarchitecture

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Specifications

- 2nd Generation Core
- Successor to Nehalem
- Released January 2011
- CPU 1.60 GHz to 3.60 GHz
- Based on x86 CISC instruction set

New for Sandy Bridge

- Turbo Boost 2.0
- New cache (L0)
- Pipelining
- Shared L3 cache
- Improved Branch prediction
- Advanced Vector Extensions (AVX)
Turbo Boost

- Automatic overclocking
- “energy credits”
- Low GPU activity

Pipelining
- 14 to 19 stages
- Load and Store
- Microinstruction cache (L0)
References

- https://en.wikipedia.org/wiki/Pentium_4
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  Named_Sandy_Bridge/links/572667f408ae262228b21030.pdf

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