Writing a RISC-V Processor
RISC-V

• Open Architecture
• Base/Extensions style ISA
  - Integer Base (I)
  - Multiply/Divide (M)
  - Atomics (A)
  - 32-bit Floating Point (F)
  - 64-bit Floating Point (D)
  - General (G) – aka. IMAFD
  - Compressed (C)
  - Vector/SIMD (V)
  - Bit Manipulation (B)
  - Etc.
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Platform

• Xilinx Spartan 6 (XC6SLX16)
• 256MB LPDDR3 Memory – Not Used (Unfortunately)
• 50MHz System Clock
• USB to Serial – Not Used (Probably)
• 24-bit RGB VGA Interface
• USB Host – Not Used
• 2 LEDs
• 2 Input Switches
• Additional connectors – Not Used
• Powered from USB or external power adapter

Thanks to Ralph Stirling for lending to me.
RISC-V Core (Planned)

- 32-bit variant of RISC-V
- 2-Stage Pipeline
  - Fetch
  - Execute
- Uses Dual-port Block-RAM
  - Only 590 Kbits (73.7 KB)
  - 20KB used for Video Output
- Should be able to run at 50MHz
- 31 32-bit Integer Registers
- Memory-Mapped I/O
- Will implement HW Multiply/Divide if time
Video Output

- 800x600 @72Hz
  - Dot clock matches system clock (50MHz)
  - Doesn’t take too much memory
- 100x75 text-based output
- 8x8 bitmap font based off of CP437 (IBM PC’s font)
- Used for debug output
- Hardware cursor tracking
- Memory-mapped if time
Software

- Write in C++14
  - RISC-V backend added to GCC 7.x
    - Supports RV32I

- Game
  - Simple text-based adventure game
  - Tic-tac-toe
  - Snake
  - Suggestions?
    - Limited controls
Previously Planned

- RV64GC
- Boots Linux
- Implemented in Cpp-HDL
  - Templates
  - Meta-programming
  - Object-oriented
  - Compiles to Verilog
  - Ran out of time (after writing 15k lines)
    - github.com/programmerjake/cpp-hdl
- May finish later
References

- https://riscv.org/specifications/
- https://github.com/programmerjake/voxels-0.7/blob/master/res/textures.png