Introduction

- What is the Atom Processor?
- The Atom processor is a microprocessor designed by Intel for use in mobile electronics where power consumption is the main limiting factor and performance is a secondary, yet still important, concern.
- Designed to try and enter into the low-power market share dominated by ARM processors.
Introduction Cont.

- The Atom Processor was developed using a new microarchitecture that was very different from Intel’s other processors.
- Three Primary Design Goals:
  1. Drastically decrease power use
  2. Powerful enough for general web use
  3. x86 compatibility

Target Markets

- Economy laptops and tablets (i.e. netbooks)
- Mobile internet devices (i.e. MIDs)
  - Mobile internet devices were a much more important demographic 10 – 12 years ago when the Atom was first being introduced
  - Most (if not all) function that MIDs specialized in are now handled by smartphones
- Pictured is Intel’s Gigabyte M528
Codename Silverthorne & Diamondville

Silverthorne (2008, MID market)

- Silverthorne was the codename for the processor which eventually became the Atom Z5xx series for MIDs.
- Diamondville became the Atom N2xx series designated for use in economy desktops and netbooks.

<table>
<thead>
<tr>
<th>Feature</th>
<th>Intel Atom Z500</th>
<th>Intel Atom Z510</th>
<th>Intel Atom Z530</th>
<th>Intel Atom Z540</th>
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<tbody>
<tr>
<td>Core freq</td>
<td>800MHz</td>
<td>1.1GHz</td>
<td>1.6GHz</td>
<td>1.8GHz</td>
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<td>FSB Freq</td>
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<td>533MHz</td>
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<td>TDP</td>
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<td>220mW</td>
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<td>Instructions</td>
<td>32bit</td>
<td>32bit</td>
<td>32bit</td>
<td>32bit</td>
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</table>

Memory

- L1 Cache:
  - 36K Instruction cache; only 32K available for use
  - 24K Data cache
    - Instruction and data cache have only 1 read port and 1 write port each
- 512K L2 Cache
- Two hardware prefetchers
Design Philosophy

- The target power consumption when designing the Atom was to be 90% lower than the Pentium M (TDP of approx. 21 W)
- Start from the ground up with a new, low power x86 core codenamed Bonnell a dual-issue, in-order core
  - Intel's other microarchitecture's such as the Pentium M or Core 2 were too power hungry to meet the design goals for the Atom Processor
- New power vs. performance design philosophy: +1% performance to +1% power consumption
  - Intel's previous design philosophy was +1% performance to +2% power consumption.

Design Philosophy cont.

- No out-of-order processing
  - Required too much power hungry circuitry with not enough performance gain
- Very little speculative decoding
- Very little instruction transformation (micro-ops)
  - Less than 4% of instructions in a typical program generate multiple micro-ops
The Bonnell Core

- Originated as a single-issue in-order core but was expanded into a 2-issue core
  - For comparison most desktop x86 processors are 3 or 4-issue
- Two paths for instructions: Slow path and the fast path
  - No speculative decoding on slow path but tags instruction for future reference
  - Fast path takes previously tagged instructions and employs some speculative decoding aided by the tag bit set by the slow path
  - Slow path processes 1 instruction every 3 clocks vs. 1 instruction every 2 clocks for the fast path
- The power penalty for incorrect speculation was too much for a battery powered device

Hyper-Threading on the Atom

- 2-way SMT
- Performance boost of 36-47%
- Power use increase of 17-19%
- Die area increase of 8%
- Gives a huge performance vs power increase of 2% performance vs. 1% power
- Bare minimum execution units to save on power
  - No dedicated integer multiplier or divider. Instead function are shared with the SIMD FP units
Power Saving States

- Uses multiple power states
- Ranges from high-performance state (C0) to ultra-low power state (C6)
- C6 state uses approx. 1.5% of TDP
- To enter C6 mode
  - Processor saves state info, stops clocks, shuts down FSB, and goes to sleep
- To exit C6
  - Clocks restart, restore the state info, and primes the pipeline
- Exiting C6 mode takes around 100us

Power Saving States Cont.

Power C-States

- Core voltage
  - C0: High
  - C6: Low
- Core clock
  - C0: ON
  - C6: OFF
- PLL
  - C0: ON
  - C6: OFF
- L1 caches
  - C0: Flashed
  - C6: Off
- L2 caches
  - C0: Flashed
  - C6: Off
- Wakeup time
  - C0: Active
  - C6: Partial Flashed
- Power
  - C0: High
  - C6: Low

C6 residency can be as high as 90% depending on Usage and Workload

Under embargo until April 1, 8:00pm US Pacific time
The end (sort of) of Atom

- In April of 2016 Intel announced 12,000 job cuts and announced plans to shift away from trying to capture the mobile market after gaining only 1% market share in 2015.
- Intel also announced the end of the Atom chip line to coincide with this drastic change in the company’s business strategy.
- More recently however Intel has revealed that the Atom line of chips isn’t dead just rebranded.
- The Joule is a system-on-a-module designed for Internet of things developers and features an Atom processor.

References

- http://www.anandtech.com